

Set	Items	Description
S1	2930223	(IP OR INTERNET() PROTOCOL OR NETWORK) () ADDRESS OR URL OR U- RLS OR (UNIFORM OR UNIVERSAL) () RESOURCE() LOCATOR? OR ADDRESS? OR LINK? ? OR NAMESPACE? OR DOMAIN?
S2	8952	(HASH OR LOOKUP OR LOOK() UP OR ROUTING OR PREFIX OR MASK) - (2N) (TUPLE OR TABLE? OR ARRAY? OR (MATHEMATICAL OR DATA) () EL- EMENT? OR MATRIX? OR MATRICES OR COLUMN? OR ROW? OR GRAPH?) OR DHT
S3	666836	(PARALLEL? OR MATCH? OR EQUAL? OR CORRESPOND? OR CONTROL? - OR PARITY OR ALIGNMENT) (2N) (SEARCH? OR QUEST? OR PURSU? OR SE- EK? OR QUER? OR MATCH? OR FIND? OR LOOK? ? OR LOOKING)
S4	8963785	DOCUMENT? OR FILE? OR OBJECT? OR PACKET? OR BLOCK? OR DATA OR MESSAGE OR E-MAIL OR EMAIL OR TEXT
S5	146589	(SECONDARY OR FURTHER OR ADDITIONAL OR NEW OR SUPPLEMENT? - OR MORE OR EXTRA?) (2N) (TUPLE OR TABLE? OR ARRAY? OR (MATHEMA- TICAL OR DATA) () ELEMENT? OR MATRIX? OR MATRICES OR COLUMN? OR ROW? OR GRAPH?)
S6	1053	(MULTIPL? OR MANY OR PLURAL? OR NUMEROUS OR SEVERAL OR DUP- PLICATE OR UNLIMITED) (2W) S5
S7	100	S1 (S) S2 (S) S3
S8	0	S7 (S) S6
S9	2	S7 (S) S5
S10	338	S2 (S) S3
S11	0	S10 (S) S6
S12	180	S10 (S) S4
S13	80	S12 (S) S1
S14	2	S13 (S) S5
S15	0	S12 (S) S6
S16	80	S7 (S) S4
S17	180	S12 OR S16
S18	72	S17 (S) (SECONDARY OR FURTHER OR ADDITIONAL OR NEW OR SUPP- LEMENT? OR MORE OR EXTRA?)
S19	72	S9 OR S14 OR S18
S20	45	S19 NOT PY>1999
S21	43	S20 NOT PD>19991213
S22	38	RD (unique items)
File 647: CMP Computer Fulltext 1988-2003/Sep W3 (c) 2003 CMP Media, LLC		
File 674: Computer News Fulltext 1989-2003/Oct W4 (c) 2003 IDG Communications		
File 696: DIALOG Telecom. Newsletters 1995-2003/Nov 03 (c) 2003 The Dialog Corp.		
File 175: Quotations Database 1979 (c) 1979 Oxford University Press		
File 15: ABI/Inform(R) 1971-2003/Nov 01 (c) 2003 ProQuest Info&Learning		
File 9: Business & Industry(R) Jul/1994-2003/Nov 03 (c) 2003 Resp. DB Svcs.		
File 810: Business Wire 1986-1999/Feb 28 (c) 1999 Business Wire		
File 624: McGraw-Hill Publications 1985-2003/Nov 03 (c) 2003 McGraw-Hill Co. Inc		
File 636: Gale Group Newsletter DB(TM) 1987-2003/Nov 03 (c) 2003 The Gale Group		
File 813: PR Newswire 1987-1999/Apr 30 (c) 1999 PR Newswire Association Inc		
File 613: PR Newswire 1999-2003/Nov 04 (c) 2003 PR Newswire Association Inc		
File 16: Gale Group PROMT(R) 1990-2003/Nov 03 (c) 2003 The Gale Group		
File 160: Gale Group PROMT(R) 1972-1989 (c) 1999 The Gale Group		
File 553: Wilson Bus. Abs. FullText 1982-2003/Sep (c) 2003 The HW Wilson Co		

22/3,K/1 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01198293 CMP ACCESSION NUMBER: EET19990816S0026
MMC, Lara team up on net processing
ELECTRONIC ENGINEERING TIMES, 1999, n 1074, PG24
PUBLICATION DATE: 990816
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News
WORD COUNT: 91

... plans to combine MMC's network processors with Lara's SuperCAM engines-which are based on content- **addressable** memories-into single-chip solutions, Lara's **new** ternary memories will be co-marketed with MMC's network processors to provide **more efficient look - up table** architectures for policy-based networking requiring multiple **parallel searches** of Internet Protocol **packet** headers, the companies said.
Copyright 1999 CMP Media Inc.

22/3,K/2 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01196007 CMP ACCESSION NUMBER: EET19990712S0032
Kawasaki rolls CAM search engine, preps classifier
Loring Wirbel
ELECTRONIC ENGINEERING TIMES, 1999, n 1069, PG38
PUBLICATION DATE: 990712
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Semiconductors
WORD COUNT: 574

TEXT:

... indicates how desperately developers of edge routers need to reduce memory costs as lookup tables for networking **addresses** grow **more** varied and complex. Kawasaki LSI USA Inc., one of the few consistent developers of CAMs since their renaissance in the early 1990s, is sampling a longest- **match search** - engine CAM based on a binary architecture, and promising fall delivery of a classification engine that uses a mixed-mode binary/ternary structure to handle a combination of **data - link** , Internet-Protocol and TCP layer search duties.

22/3,K/3 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01155677 CMP ACCESSION NUMBER: EET19980316S0088
Flexible CPUs needed for diverse apps
Syed S. Hussain, MiniRISC Product Manager, Kevin Daberkow, Project Leader, Consumer Products Division, Dan Vogel and Victor Helenic, Field Applications Engineers, LSI Logic, Milpitas, Calif.
ELECTRONIC ENGINEERING TIMES, 1998, n 998, PG100
PUBLICATION DATE: 980316
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Embedded Systems
WORD COUNT: 1654

... further.

Not only are the processing requirements of these systems increasing, but also the width of the **data** to be processed. The next generation of routing products will be implementing Internet Protocol

version 6 (IPv6...

...IP next generation (IPng, designed to take an evolutionary step from IPv4). Changes include expanded routing and **addressing** capabilities by increasing **IP address** size from 32 to 128 bits. That will support **more** levels of **addressing** hierarchy and a greater number of **addressable** nodes, as well as a simpler auto-configuration of **addresses**. With current 32-bit machines, four accesses are required to pull in an IPv6 **address**. Then, those **addresses** are routed to a content-**addressable** memory (CAM) or into a **lookup table** to **find a match**.

Therefore, each **match** requires multiples of four accesses. However, with a 64-bit-wide processor, only two accesses are required, which translates into increased bandwidth and lookup speeds. Greater throughput is also demanded. **More** and **more**, traditional 10-Mbit Ethernet is giving way to 100-Mbit Ethernet, and, in some cases, gigabit Ethernet...

...DS3 traffic at 55 Mbits/second on the wide-area network (WAN) are being implemented. These higher **data** throughputs require correspondingly higher control-processing capabilities by the embedded processor.

Within the remote-access paradigm, the...

22/3,K/4 (Item 4 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01140196 CMP ACCESSION NUMBER: CRN19971006S0143

Fighting Fire With Fire:Internet Security
COMPUTER RESELLER NEWS, 1997, n 757, PG143
PUBLICATION DATE: 971006
JOURNAL CODE: CRN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: White Paper:Cheyenne
WORD COUNT: 6300

... address comes by, the device sends it to that address. If it finds no match with an **address** in the internal table, it permits the **packet** to continue through the network). Routers are smarter than bridges, allowing logical **links** of separate networks. The intelligence in the router can be used to reroute traffic in case some...

...find, moment -by-moment, the lowest-cost routing of traffic from one point to another. Routers become **more** appropriate than bridges as your network grows in size or complexity. With routers, you can create a mesh topology-a large, complex system offering several paths between any two points. Mesh topologies are **more** fault-tolerant than other topologies, but potentially **more** difficult to secure. The greater intelligence of routers has some drawbacks, of course. By examining each **packet** before sending it on, **packet** processing with routers can be slower than **packet** processing with bridges. Intelligence also has its price:You pay **more** for routers than for bridges.

Routers are normally one-way filters, whereas many bridges don't filter...

22/3,K/5 (Item 5 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01023772 CMP ACCESSION NUMBER: NWC19940404S3529

Choose The Right Dial-Up Router For You (Routers)
Dave Molta and Jenny Gluck
NETWORK COMPUTING, 1994, n 504, 150
PUBLICATION DATE: 940404
JOURNAL CODE: NWC LANGUAGE: English
RECORD TYPE: Fulltext

TEXT:

... hold significant appeal as tools for providing temporary network connections and as backup devices for higher-speed **links**, particularly wireless **links** that may be affected by adverse weather conditions. Although most popular products provide a core set of basic features, **matching** your requirements to the available alternatives can be challenging. This Buyer's Guide provides an overview of the **more** significant questions to ask vendors, along with recommendations of how to weigh features when making your final...

...protocol suites do I need to support? Will the company and/or site grow enough to require **additional** lines with load-balancing algorithms (inverse multiplexing)? Will it be cheaper, or possible, for the dial-up...

...bandwidth and multiple lines are desirable, can the router monitor traffic levels dynamically and open or close **additional** connections? Are specific features limited to a selected protocol, such as Internet Protocol (IP)? All About Protocols...

...need IP access only or are willing to tunnel other protocols inside IP, a number of alternative, **link**-level protocols are available, including the Point-to-Point protocol (PPP), the Serial Line Internet Protocol (SLIP)...

...PPP is chosen most often. PPP's advantages include a method for encapsulating datagrams using high-level **link** control over asynchronous or synchronous serial **links** and a comprehensive **Link** Control Protocol (LCP) used to establish, configure and test the **data** - **link** connection protocols and to define the different network-layer protocols. Support for PPP also facilitates interoperability among...

...case. You may be disappointed to learn that the routing protocols available in dial-up routers are **more** limited than those found in high-end routers. The most common routing protocol for IP is the...

...a combination of its own RIP and the Service Advertising Protocol (SAP). AppleTalk Phase 2 uses the **Routing Table** Maintenance Protocol (RTMP), the Zone Information Protocol (ZIP) and the Name Binding Protocol (NBP). Unlike traditional routers...

...proxy networks in which an algorithm is designed to buffer the routers from the changes in the **routing tables**. Spoofing is used between local and remote networks. When a modem disconnects from a NetWare server, users...

...the router to its routing information. The dial-up router must be updated with changes in the **routing table**. There must be a method, such as proxy networks, to discern valuable information to minimize operating costs...

...letting the router do the rest, or as complex as assigning an internal network number and IPX **address**. Most dial-up routers support the full AppleTalk protocol implementation, while others support the AppleTalk Remote Access **more** limited **packet** - filtering capabilities and pass broadcast and multicast **packets** across the LAN. This can be troublesome over low-bandwidth **links** using chatty protocols, such as IPX and AppleTalk, since a significant portion of the limited bandwidth is not available for the transmission of meaningful **data**. Modems and Connection Some routers come with internal modems, while others provide a serial interface that must...

...sense to ask vendors about upgrades. Many products allow for multiple WAN interfaces for example, two or **more** dial-up circuits that can be pressed into service automatically if traffic warrants. If the need for...

...s wise to ask about products that support ISDN Basic Rate Interface (BRI) and Switched 56.P **Data** compression facilities are very important, particularly for applications in which large numbers of **text files**, such as e-mail messages, will be carried across the **link**. In addition to the compression found in CSLIP or PPP, compression can be implemented in either the...

...V.42bis or MNP v5 and/or the proprietary router hardware. When planning for future growth or **additional** bandwidth needs, ask your vendor whether the serial connection can handle speeds up to 115.2 Kbps. This should allow ample room for growth as **new** modem technologies, such as V.FAST, are introduced. Most vendors will handle maximum speeds of 57.6Kbps...
...and Setup Many sites will be concerned about security, since these products use industry-standard modems and **link** protocols. Most products incorporate multiple security mechanisms ranging from password-based authentication to dial-back security. Protocol...

22/3,K/6 (Item 6 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2003 CMP Media, LLC. All rts. reserv.

01022154 CMP ACCESSION NUMBER: WIN19940601S1885
Mobile Mail Keeps Remote Users in the Loop (E-Mail Software)
Hailey Lynne McKerry
WINDOWS MAGAZINE, 1994, n 506 , 076
PUBLICATION DATE: 940601
JOURNAL CODE: WIN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: New Products

TEXT:

... location profiles, which can be altered with a single mouse click, to connect from often visited destinations. **More** than 40 location icons (hotel, home, office, cities, countries) ship with the product; you can also add...

...UNIX) and X.25. cc:Mail Mobile also supports connections via ISDN, PBX, direct connection, RAM Mobile **Data**, cellular and landline modems. The package includes scripts for **more** than 70 popular modems and supports background operation. A preview function lets you gather information about incoming...

...Technology, the prior interface was transitional, to provide support for both DOS and Windows users. In the **new** version, a button bar has been added to the pop-up menus. The bar includes icons for...

...boxes, resizable windows and the ability to select your own fonts. The Speed Read function automatically tags **new** messages and displays the first **message** upon sign in. You can display incoming and out- going messages side by side. Network 3.0...

...off- site with PC or laptop using Portable Mail for Windows. The software can download UNIX mail **files** so you can display, save, answer and manipulate mail using the Windows GUI. The interface includes an...

...actions are automatically reconciled. You can create a remote post office on any Windows computer, then transfer **files** with transfer software or via a diskette. You can perform mail functions, including printing and saving messages...

...Because it has full OCR functionality, FaxWorks Pro LAN does not require you to retype received faxed **documents**. It has personal and shared telephone books, logs and **file** cabinets. FaxTracker, the program's **document** retrieval and storage tool, brings up a **document** log that lists scheduled and concluded faxes. FaxTracker can also display the results of a search and provides specific fax information, such as the

file name, type and size. FaxWorks Pro LAN features automatic Group 4 compression and supports up to eight...

...converts a fax machine into a scanner or local printer. With the FaxConverter, you can scan a **document** into your PC or print **documents** on your fax machine. DataFax+'s optical character recognition (OCR) engine transforms scanned **documents** into editable **text**. In the **new** version of DataFax+, the OCR engine features improved ligature recognition ...and Type Reader 1.0. The DataFax software includes a Captive QuickFax icon which lets you clip **data** from an application, add a fax **address** and send it. The Smart Dialing feature lets you add country, area and long distance dialing codes...

...Contact: Trio Information Systems Inc., 800-880-4400 919-846-4990 Circle Inquiry 563 RightFAX Supports Binary **File** Transfer Binary **file** -transfer support, which allows **files** to be faxed as editable **documents**, has been added to RightFAX 3.5 fax server software. The software lets multiple users on Novell...

...directly from e-mail systems. RightFAX includes a drag-and-drop feature that allows you to send **files** as either fax **documents** or binary **data files** by dragging them onto an icon or window. With the RightFAX OCR module, available for \$1,195...

...faxes on the basis of key words found on the fax's cover page. You can build **routing tables** to direct the fax to the recipients with one of several keywords associated with that user. If...

...with One Program Time Planner Deluxe 2.0 bridges the gap between PIMs (for tracking names and **addresses**) and project management systems (for tracking project deadlines and resources). The program is designed for task-oriented...

...increments (five minutes or longer), as well as view a graph of allocated costs over time. The **address** book accommodates three **addresses** and six telephone numbers per entry, and includes an autodialer. You can also place information in folders...

...to a folder for automatic assignment to the appropriate folder on the basis of the note's **text**. Time Planner Deluxe 2.0 Price: \$129; until June 30, \$59 Contact: H.M. Hinsch & Co., 800...

...568 Commence Keeps Customer Contacts Current The latest upgrade of the Commence contact manager is highlighted by **more** than 15 **new** features, including e-mail interfaces and a **more** powerful search capability. Version 2.1 retains familiar features, including the **address** book, appointment calendar, note keeper, to-do and task list manager and travel expense tracker. The **new** version adds the ability to send e-mail using Commence's Agent technology. Messages can be sent...

...on a report, or for resizing rows and columns with the mouse. Commence can now play sound **files** or video clips when a predefined situation occurs. The **new** version also adds user interface features, such as direct appointment entry in the calendar view, maintenance of...

...4666 Circle Inquiry 569 Software Ties Up Contact Management Loose Ends CrossTies 1.0 uses patent-pending **object** - oriented technology to manage information. The program lets you assign a name of up to 256 characters in length to an information item, then **link** that information to other types of **data** and view all related items on a single screen. You can drag and drop information between related elements (people, **documents** or activities) or use the QuickLink button to associate different types of information. CrossTies can store and...

...a notes field. You can define templates to prefill fields with standard information and place frequently used **objects** on the "Shelf" for quick access. The Trail button allows you to access your most recent work...

...of upcoming events and prints daily, weekly and monthly calendars. A

built-in viewer lets you view **documents** from a variety of programs. CrossTies 1.0 Price: \$149 Contact: CrossTies Software Corp., 800-955- TIES, 214-407-9996 Circle Inquiry 570 Business Productivity Tools Automate Repetitive **Document** Production HotDocs helps you build intelligent templates using Word (versions 2.0 and 6.0), WordPerfect (5.2 and 6.0) and Ami Pro (3.0) **documents** . The templates ...the user to fill in the blanks. The program automates the production of repetitive, routine word processing **documents** from business letters to loan agreements by letting you identify **text** that will change with each **new document** (such as dates, names, adverbs or pronouns) and replace it with a variable. To assemble a **document** using a finished template, you simply click on a button. The tem- plate asks questions based on the user- defined variables and inserts the **new** information. You can specify formats for the variables, so that information is displayed in the correct format...

...The program includes options to replace pronouns (his/her) with the proper gender , and can conditionally replace **text** . HotDocs 1.0 Price: \$99; introductory price, \$49 Contact: Capsoft Development Corp., 800-500-DOCS, 801-375-6562 Circle Inquiry 571 Software Simplifies Employee Evaluations Two **new** software packages offer help to managers faced with the difficult task of conducting and **documenting** employee performance reviews. Austin-Hayne's Employee Appraiser using a " writing by example" approach, presents a series...

...it finds potentially troublesome language , the software offers possible alternatives. The program's Manager's Notebook helps **document** important events on a day- to-day basis for inclusion in later reviews. Avantos Performance Systems' Review...

...a Quick Build mode that leads the review writer through questions that gather key information and a **Document** mode for **more** experienced users. Users click on icons to get help in specific areas. The program can import goal and performance information from Avantos' ManagePro, an employee management program. Review Writer can also incorporate comments on **objectives** and performance recorded in ManagePro. The program can suggest actual **text** , prompting users to agree or disagree with statements about a performance area or skill. The writer can select all, some or none of the generated review **text** . The program includes predefined sample templates for general job titles, such as managers, team leaders and customer...

...you can select a sample letter , then use the program's hints to help you produce professional **documents** for different situations. ViewWorks' Find function searches **documents** for keywords or phrases, and the built-in word processor lets you customize a selected **document** , then send the **text** to your own word processor for **further** editing. Business LetterWorks includes 400 letters covering customer relations, credit and collections, personnel relations, internal communications, community...

...version of its Managing Your Money (MYM), to help you manage your banking, investments and taxes. The **new** version adds a SmartDesk graphical navigator. The SmartDesk appears on-screen as a picture of a traditional office setting, complete with desk, bookcase, **file** cabinet and windows. You can access any program feature by clicking on items in the picture. SmartDesk comes with preset defaults that **link** standard Windows applets, such as Calendar, Calculator and Notepad, to the appropriate SmartDesk icons. Or you can...

...and annual appreciation and yield; MYM also tracks cost, price changes, risk levels, liquidity and other investment **data** . The SmartPlanner analysis function helps users think through financial questions like Should I buy or lease? or...

...the highest priority debt. The loan consolidation schedule feature combines all your current debt information into one **new** loan. Interest rates are configurable as daily, monthly, APR (annual percentage rate) ... by percentage and commission plus base pay. The software allows you to

process bonus pay and electronically file direct deposits. It can also be configured for multiple pay periods and allows unlimited benefits, deductions, additions...

...787-7287, 208-336-2555 Circle Inquiry 587 HELP AUTHORIZING SOFTWARE Word Add-On Automatically Generates Help Files HelpBreeze 1.6, a Windows help authoring add-on, has been upgraded to include a Topic Wizard...

...list of topics, choose a format, and the Topic Wizard tool automatically structures and formats your help file. It expands your list into fully formatted topics and inserts them into the help document. Topic titles, context strings, keywords and browse sequences are created. The add-on works with Microsoft Word...

...1.6 provides point-and-click support for all Windows 3.1 Help system features (such as secondary windows and help macros). HelpBreeze also offers automated two-way conversion between electronic and printed versions of documents, and support for creating context-sensitive help. Slide Show, a distributable DLL, allows you to include animation, slide shows with VCR-style controls, sound and 256-color graphics within help files. The Slide Show add-on requires a Windows resource editor, such as Borland Resource Workshop or Microsoft...

...6 Price: \$279 Contact: Solutionsoft, 408-736-1431, fax 408-736-4013 Circle Inquiry 581 Make Help Files the Easy Way Doc-To-Help 1.6, a new version of the help authoring tool, includes Hyperformance Tools utilities that assist in the creation, viewing and distribution of hypertext help files. The Doc-To-Help Navigator, one of the new tools, displays the structure of a help file in expandable outline form. You can use it to browse the help file, then jump to any topic in the file through a hypertext link. You can also select and print multiple topics from the Navigator. Other Hyperformance tools allow you to drag and drop help files into Visual Basic, and add 256-color bitmaps and watermarks to your help files. Any bitmap can be made into a background watermark and displayed, either centered or tiled, in the...

...Price: \$295 Contact: WexTech Systems Inc., 800-WEX-TECH, 212-949-9595 Circle Inquiry 582 Create Help Files in Word or Ventura Publisher MasterHelp lets you generate Windows help files from text created in Microsoft Word or Corel Ventura Publisher. The result is a finished help file that includes hypertext jumps, pop-up screens, secondary windows and browse sequences. MasterHelp also automatically creates Microsoft Multimedia Viewer files. You control the design of your help files by specifying template fonts, graphics, tables and indentation. The program automatically creates a table of contents in a secondary window, as well as a pop-up window with an overview of the entire document or the current chapter. The Help search facility is loaded with all the topics in your document. An interactive hypertext editor with special macros lets you add extra hypertext jumps. You can convert topic names contained in the text into hot buttons that jump to that topic. You can also create "see also" pop-up listings on additional topics and tag words for inclusion in the search table. MasterHelp Price: \$495 Contact: Performance Software Inc...

...and rerun procedures and analyses without having to create macros or specialized code. The StatFolio feature saves file and variable names, graphics settings and analysis options so that the same analysis can be run on a new data set. The program includes a DDE link to Excel, Lotus 1-2-3 and Quattro Pro. Changes in a linked spreadsheet are automatically...real-time news on FM radio (in a dozen major U.S. cities) and by satellite (in more remote areas) to a receiver attached to the PC's serial port. Mainstream Newscast software receives and displays stories from the news services to which you subscribe. More than 150 information services including Associated Press, Reuters, Market News Service, PR Newswire, Business Wire and Federal...

...windows according to topic. Mainstream Newscast Price: Software, \$995;

FM receiver, \$495; satellite dish, \$990 Contact: Mainstream Data Inc., 801-584-2800, fax 801-584-2831 Circle Inquiry 589 Are You Sick of Flying Toasters...

...and-drop visual programming environment. The resulting screen saver can run either as a single DOS executable file or under Bourbaki's A Touch of Chaos Windows, which comes with ForShow. The program supports a variety of formats, including .BMP, .GIF and .PCX. It also handles .WAV and .VOC sound files, Autodesk Animator (.FLI and .FLC) files and its own fractal file format for graphics. You can set transition effects including venetian blinds, diagonal, drip, explode, spiral, split, weave ...

...is done, you can run complete shows or selected portions. ForShow also provides an icon-based visual file management system for organizing slide-show elements. ForShow 1.0 Price: \$79 Contact: Bourbaki Inc., 800-289-1347, 208-342-5849 Circle Inquiry /headline 590 Development Tool Sports Enhanced VB Links Develop client/server applications faster with SQLWindows 4.1, a new version of the SQL application development environment. Version 4.1 adds seamless support for Visual Basic custom controls (.VBX files), Windows classes and business graphics. The upgrade offers improved operation with Oracle 7.0 server databases. You...

...Oracle-stored procedures for queries and updates and use the Oracle array interface. SQLWindows also offers tighter links to two leading computer-aided software engineering tools: Popkin System Architect and LBMS Systems Engineer. The corporate...

...be fed directly to the board. It supports Microsoft Video for Windows and can play .WAV audio files. The board is modular so that it can be upgraded by adding a more powerful compression engine. MovieMan ships with the Adobe Premiere multimedia authoring system, as well as Logitech's ...

...Logitech's EasyClip, a capture utility that allows for drag-and-drop integration of captured images into documents created by OLE-compatible devices. MovieMan Price: \$299 Contact: Logitech Inc. 800-231-7717, 510-795-8500...

...different adjustments to the monitor including raster rotation, pincushion and trapezoid (phase) control and color calibration to match Pantone and device output color samples, are mounted at the front of the monitor. A bezel-mounted...

...kits include a double-speed CD-ROM drive with a 320ms average access time and a 300KBps data-transfer rate. A Media Vision 16-bit sound card with 16-bit stereo recording and playback at...

22/3,K/7 (Item 1 from file: 674)
DIALOG(R)File 674:Computer News Fulltext
(c) 2003 IDG Communications. All rts. reserv.

079205

3Com eyes e-business, CoreBuilder 9000 is key

Byline: Jim Duffy

Journal: Network World

Publication Date: November 03, 1999

Word Count: 761 Line Count: 76

Text:

... But the key platform on which e-Networks will be based is 3Com's CoreBuilder 9000 enterprise data center switch."We have a full commitment to this platform," says Edgar Masri, senior vice president of...

... rumors spread by competitors that 3Com was not backing the big switch. Some customers have gotten the message. U.S. Xpress, the fifth

largest publicly traded **load** carrier, just spent \$1 million on a Gigabit Ethernet e-Network based on 3Com's CoreBuilder 9000. "Their vision of e-commerce **matched** our own," says Norman Thomas, vice president of information services at U.S. Xpress. The e-Networks strategy is based on three building **blocks** : applications, access and availability. Applications refers to the infrastructure for supporting e-business applications, such as the...

... redundant components within the 3Com product line to ensure application uptime and no single point of failure. **New** products to support this strategy include an eight-slot version of the CoreBuilder 9000 switch for wiring closet, backbone and **data** center applications (NW, Sept. 20, page 12). The **new** switch offers all of the redundancy of the 16-slot CoreBuilder 9000 but half the port density...

... sport four Gigabit Ethernet ports, provide wire-speed IP and IPX routing and switching at 8 million **packet** /sec, and feature 802.1p **packet** tagging for prioritization and quality of service (QoS). The modules enable the CoreBuilder 9000 to support from...

... 56 Layer 3 Gigabit Ethernet ports in the eight- or 16-slot chassis, respectively. 3Com also announced **new** software for the CoreBuilder switches. Version 3.0 of CoreBuilder software adds 802.1p **packet** tagging for priority and QoS, the Virtual Router Redundancy Protocol for **routing table** backup, and MultiPoint **Link** Aggregation for building fault tolerant **links** between switches. 3Com says the CoreBuilder 9000 will be enhanced over the next year to support network...

... and consistent availability of network services for e-business applications. The collaboration is expected to result in **new** 3Com Transcend policy management software. This software will be rolled out in 2000 and will enable a...

... applications such as enterprise resource planning, supply chain management with business partners and relationship management with customers. **New** e-Network services, such as voice and streaming video, also require this level of management, 3Com says...

22/3,K/8 (Item 2 from file: 674)

DIALOG(R) File 674:Computer News Fulltext

(c) 2003 IDG Communications. All rts. reserv.

077600

feature

We put Gigabit Ethernet switches from seven vendors through their paces.

For the most part, the products worked well together.

Byline: ANN SULLIVAN

Journal: Network World Page Number: 81

Publication Date: September 13, 1999

Word Count: 2074 Line Count: 203

Text:

... during the test, which was conducted by The Tolly Group and Network World at a hotel in **New** Jersey. Take Lucent's Jeff Tabor, for example. Even when Lucent's boxes weren't being tested...

... were helping out each other. Nortel Networks was collaborating with Cabletron. There was Cisco breaking out its **new** enhanced spanning tree feature in front of IBM, Lucent and others. Of course, in interoperability tests, one...

... deviate from the standards so much that interoperability suffered. For customers, this means you can mix and **match** vendors depending on your deployment needs. All the switches will negotiate speed and duplex settings to maximize...

... confirmed that throughput remained within an appropriate range as we

transmitted a stream of 1,518-byte **packets** from Netcom Systems' SmartBits to each switch. We expected all the boxes to pass, and they did...

... them (see story, page 82). We wanted to determine how each switch acts upon receiving a control **message** - whether a switch passes along the **message**, throttles back traffic or modifies traffic on a port-by-port basis. Different implementation strategies yield different...

... at one switch's output port and watched to see if that switch initiated a flow control **message** to the other switch. We then queried the receiving switch to see if it received the control **message**. Using network analyzers - Network Associates' Sniffer Pro High-Speed for the gigabit **links** and Wavetek Wandel Goltermann's DominoFE for the Fast Ethernet **links** - we verified whether traffic flow from the switch that got the pause **message** was reduced until congestion was clear. We performed the tests in both directions with each pair. Four... Protocol (RIP) Versions 1.0 (mandatory) and 2.0 (optional) Description: Each switch pair must exchange IP **routing table** information in compliance with RIP Version 1.0 and, optionally, Version 2.0. Degree of difficulty: Low Participants...

... didn't configure their switches with static route entries but instead allowed the switches to build dynamic **routing tables** based on exchanged RIP information. We required each switch pair to update their **routing tables** correctly with network information from the remote networks and made sure that pairs of TCP/IP end...

... don't support static IPX routing. Test 6: IPX RIP (optional) Description: Each switch pair must exchange **routing table** information in compliance with IPX RIP. Degree of difficulty: Low Participants: Layer 3 switches Results: All participants passed. To...

... participants did not configure their switches with static route entries but instead let the switches build dynamic **routing tables** based upon exchanged RIP information. We required each switch pair to update their **routing tables** correctly with network information from the remote networks and again made sure that pairs of IPX end stations running Ganymede's Chariot could communicate across the network. Test 7: **Link** aggregation (optional) Description: Each switch pair must interoperate over a single aggregated **link** consisting of two full-duplex, Fast Ethernet **links**. Degree of difficulty: Moderate Participants: All except IBM's 8275-416 Ethernet Switch Results: All participants passed. All the vendors tested have developed **link** aggregation schemes that let you bundle multiple point-to-point **links** to create a single logical **link** of greater bandwidth; Cisco's Fast Ether-Channel, Lucent's OpenTrunk and Cabletron's SmartTRUNK are a...

... we didn't verify compliance with any particular specification, such as the IEEE's pending 802.3ad **Link** Aggregation Protocol. Nonetheless, we wanted proof that proprietary trunking solutions can work in a multivendor environment. To test **link** aggregation, we set up pairs of switches connected by a single aggregated **link** consisting of two full-duplex Fast Ethernet **links**. We generated 1,518-byte **packets** from a pair of SmartBits ports to two nonaggregated "feeder" ports on each switch and checked to see that each switch then forwarded traffic to its mate across an aggregated "trunk" **link** at a rate that exceeded the bandwidth of a single **link**. That is, we ensured the system forwarded **more** than 100M bit/sec in each direction across the trunk. Only IBM's 8275-416 Ethernet Switch doesn't support **link** aggregation. The other 11 switches participated, and all passed. Test 8: Accelerated convergence (optional) Description: Each switch...

... developed proprietary accelerated convergence systems. These systems purport to speed the recovery process in the event a **link** fails. The systems are typically a replacement for the 802.1d Spanning Tree Protocol in Layer 2...

... three seconds. But it seems vendors aren't as confident in this arena as

they are with **link** aggregation. Only two vendors accepted the challenge. We connected two of Cisco's Catalyst 2948G switches and...

... mesh so each switch from Cisco connected to both switches from Nortel and vice versa, yielding four **links**. We then disconnected the active **link** for each vendor and verified, using ping, the reconvergence time was less than three seconds. Test 9...

22/3,K/9 (Item 3 from file: 674)
DIALOG(R)File 674:Computer News Fulltext
(c) 2003 IDG Communications. All rts. reserv.

071828

Exposing the deep, dark secrets of TCP/IP

Byline: BRAD TURNER

Journal: Network World Page Number: 33

Publication Date: February 01, 1999

Word Count: 694 Line Count: 62

Text:

... basic workings, that is, how routers and Layer 3 switches act upon IP information to move Ethernet **packets** across the network. As a point of reference, bear in mind that IP is a member of...

... end connectivity. IP, located one layer down, at the OSI network layer, or Layer 3, communicates the **addresses** of each **packet**'s sender and receiver to the routers along the way. Routers and Layer 3 switches can read IP and other Layer 3 protocols. This information, combined with **routing tables** and other network intelligence, is all it takes to get across the room or around the world via TCP/IP. The routing process begins with an **IP address** that is unique to the sending endstation. Endstations may be assigned permanent **IP addresses** or they may borrow them as needed from a Dynamic Host Configuration Protocol (DHCP) server or other service. Each **packet** carries a source **address**, which under current (IPv4) specifications is 32 bits long. In its header, each **packet** also carries the **IP address** of the final destination. If the sending endstation determines that the destination **address** is not local, the **packet** goes to a first-hop router, typically one that is close and has been pre-assigned to the sender. Decisions, decisions. The router inspects the **packet**'s **IP address** and performs a **route table lookup** to see if the destination endstation resides on the local (physically connected) network, typically called an IP...

... An IP subnet usually is assigned to each of the router's network interfaces. If the destination **IP address** is local, the router searches an internal store of **IP addresses** and local-device media access control (MAC) **addresses**. This store is known as the **Address Resolution Protocol (ARP) cache**. ARP is the universal tool for **matching IP addresses to MAC addresses**. If the destination's **MAC address** appears, the router installs that **MAC address** in the **packet** header (removing its own **MAC address** because that's no longer needed) and sends the **packet** to the destination endstation. In the event that the destination **MAC address** does not appear in the ARP cache - it might have timed out, for instance - the router must broadcast an ARP request to the subnet referenced by the **packet**'s destination **IP address**. The endstation with that **IP address** responds, sending back its **MAC address**. The router updates its cache, installs the new **MAC address** into the **packet** header, and launches the **packet**. If the **route table lookup** shows that the **packet** is destined for a nonlocal subnet, the router forwards the **packet** to the next-hop router using the next-hop router's **MAC address**. **Routing tables** are continuously built and rebuilt by intelligent discovery protocols, such as Routing Information Protocol or Open Shortest Path First. Each router's **routing table** shows the best route to the destination **address**; for **addresses** that may be several hops away, it shows the best next-hop router. The next-hop router then performs its own **route table lookup**. If the **packet** destination is not local, it sends

the **packet** to the next hop router. If it is local, the router searches its own ARP cache for the endstation MAC. And if it doesn't find the MAC **address**, the router broadcasts an ARP request to its local subnets. This process is repeated until the **packet** reaches its ultimate destination. One danger that exists in multihop transmissions involves the creation of infinite loops, where a misconfigured router sends the **packet** back to a router through which it's already passed. To guard against infinite loops, IP includes a time to live (TTL) function, which sets a time limit for how long the **packet** can traverse the net. With each hop, a preset TTL value is devalued by one; if that number reaches zero, the **packet** is dropped and the router notifies the originator via an administrative Internet Control **Message Protocol message**. Turner is a technology marketing manager in 3Com's Large Enterprise Division. He can be reached at...

22/3,K/10 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

01514356 01-65344

Fighting fire with fire: Internet security

Anonymous

Computer Reseller News n757 PP: 143-152 Oct 6, 1997
ISSN: 0893-8377 JRNL CODE: CRN
WORD COUNT: 6357

...TEXT: address comes by, the device sends it to that address. If it finds no match with an **address** in the internal table, it permits the **packet** to continue through the network). Routers are smarter than bridges, allowing logical **links** of separate networks. The intelligence in the router can be used to reroute traffic in case some... find, moment-by-moment, the lowest-cost routing of traffic from one point to another. Routers become **more** appropriate than bridges as your network grows in size or complexity. With routers, you can create a mesh topology—a large, complex system offering several paths between any two points. Mesh topologies are **more** fault-tolerant than other topologies, but potentially **more** difficult to secure. The greater intelligence of routers has some drawbacks, of course. By examining each **packet** before sending it on, **packet** processing with routers can be slower than **packet** processing with bridges. Intelligence also has its price: You pay **more** for routers than for bridges.

Routers are normally one-way filters, whereas many bridges don't filter...

22/3,K/11 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

01423076 00-74063

A user's perspective: Software automation can deliver breakthrough results

Maxfield, David; Carmichael, Edward

Telemarketing & Call Center Solutions v15n9 PP: 30-33 Mar 1997
ISSN: 0730-6156 JRNL CODE: TLM
WORD COUNT: 1474

...TEXT: routing into the main queue. In the future, we may apply IIR capabilities to any number of **data** conditions and business rules, to do **further** intelligent routing of that call.

Our average call consists of a twominute wait plus four minutes of...

22/3,K/12 (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

01103862 97-53256

The problem of being permanent

Bradner, Scott

Network World v12n36 PP: 19 Sep 4, 1995

ISSN: 0887-7661 JRNL CODE: NWW

WORD COUNT: 649

ABSTRACT: The IPng process was initiated to **address** concerns that the 32-bit IPv4 **address** space on the Internet would be exhausted. The concept of Classless Inter- **Domain** Routing was approved to: 1. permit the assignment of **blocks** of Internet Protocol (IP) **addresses** sized to **more** closely **match** the needs of an organization so that **addresses** would be **more** efficiently used, and 2. enable the aggregation of routing information from multiple organization so that the growth of **routing tables** could be slowed. IPng does not, by itself, change the dynamics of **routing table** growth. It seems the best way to moderate growth in **routing tables** is to request, but not require, that organizations renumber their networks to **match** their **new** place in the network topology when they connect to a **new** provider.

22/3,K/13 (Item 4 from file: 15)

DIALOG(R)File 15:ABI/Inform(R)

(c) 2003 ProQuest Info&Learning. All rts. reserv.

01056016 97-05410

An industrial model based computer vision system

Magee, Michael; Seida, Steven

Journal of Manufacturing Systems v14n3 PP: 169-186 1995

ISSN: 0278-6125 JRNL CODE: JMY

WORD COUNT: 10707

...TEXT: each other will have error limits specified by the operator.

The fundamental mechanism by which these design **objectives** are met is to perform feature **matches** on a breadth-first basis such that a combination of three features from an unknown sample (image), forming a feature triad, is rapidly compared with triads from the known model(s) using a **lookup table**. The purpose of this comparison is to eliminate from **further** consideration any observed combination that does not appear as a valid feature triplet in one or **more** of the models. On the other hand, the search does not eliminate from **further** consideration any combination that, due to chance alignment of observed features, could **match** a model triad.

This preliminary matching of triads is followed by accumulating evidence for a specific model...3.2.2

The next step is to use each of these triads to index into the **lookup tables** and determine to which model triplets the triad may correspond. Of course, many of the indices generated will map to locations in the model **lookup table** that were never entered when it was constructed because many of the corners are false; however, for...

... required by the algorithm to produce the transformation. Hwang's algorithm will be used again later when **additional** features augment instantiation sets such that there are **more** than three **matches**. The output of the procedure is a set of five parameters, which are scaling factors, S_{sub} ...

... current application because some poses may not be allowed. For example, if it is known that all **objects** to be **matched** by a particular model do not vary in size, then both $S_{sub\ x}$ and $S_{sub\ y}$ should be close to 1.0. If the orientation of **objects** as they might appear on a conveyor is restricted, then $\Theta_{sub\ z}$ may be similarly constrained...for each comparison.

The model-based vision approach, however, accelerates processing by (1) employing a very fast **table lookup** mechanism based on features that may be found based on simple algorithms and (2) constraining the search for other features based on high confidence **matches** of instantiated feature sets. Table lookups based on **extracted** feature triplets are extremely fast. Problems of computational complexity generally associated with ROI and cross-correlation are reduced because subsequent feature searches are **more** restricted within the image. For example, in Figure 8b, if it were desired to search for a particular colored square region (top of an integrated circuit), once the **object**'s pose has been determined as shown in Figure 8c, it would be simple to rotate and...

... correlate it with the original image. With respect to conventional non-MBV systems, this therefore eliminates the **additional** computation required to generate multiple rotated, scaled, and translated templates that must be correlated separately across the...

22/3,K/14 (Item 5 from file: 15)
DIALOG(R) File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

00666789 93-16010

High-end project managers

Heck, Mike

InfoWorld v15n5 PP: 59-70 Feb 1, 1993

ISSN: 0199-6649 JRNL CODE: IFW

WORD COUNT: 10554

...TEXT: categories to a resource, and eight code categories to an activity. We formatted the code category to **match** a specific WBS structure. We also created a **lookup table** to **further** ensure **data** consistency.

The package includes both Gupta Technologies Inc.'s SQLTalk/Windows and Quest for Windows for ad...

22/3,K/15 (Item 6 from file: 15)
DIALOG(R) File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

00656721 93-05942

Will We Need All This Bandwidth?

Gantz, John

Networking Management v10n13 PP: B17-B18 Dec 1992

ISSN: 1052-049X JRNL CODE: TPT

WORD COUNT: 1145

ABSTRACT: Forecasts from International **Data** Corp. predict that by 1996:
1. frame relay carrier revenues will reach \$1 billion, 2. the installed
...

... cards will reach 35,000, and 3. US carrier revenue from SMDS will be \$200 million. Available **data** bandwidth is expected to grow tenfold. Reasons that user organizations should be able to use that bandwidth include: 1. The amount of computer power will grow by a factor of 20. 2.

New operating systems will fuel **new** application demand that takes advantage of 32-bit **data** paths. 3. Intel's 32-bit chip, the Digital 64-bit chip and RISC chips will be ready for **new** computing tasks. 4. Computer-to-computer traffic in support of **new** technologies will increase. 5. Multimedia and groupware applications will be into their 2nd generation. Broadband architecture will rescue corporations entangled in rationalizing multitudinous **routing tables**, linking disparate directories, and trying to keep up with station moves and real-time changes in device configurations. **Matching** user needs with actual products will be difficult since both users and vendors are treading on **new** ground.

22/3,K/16 (Item 7 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

00616926 92-32028

Parallel Database Systems: The Future of High Performance Database Systems

DeWitt, David; Gray, Jim

Communications of the ACM v35n6 PP: 85-98 Jun 1992

ISSN: 0001-0782 JRNL CODE: ACM

WORD COUNT: 9579

...TEXT: sort-merge join. It has linear execution cost rather than $n \log(n)$ execution cost, and it is **more** resistant to **data** skew. It is superior to sort-merge join unless the input streams are already in sorted order...

... corresponding partition of table relation B is scanned, and each tuple is compared against the main-memory **hash table** for the A partition. If there is a **match**, the pair of tuples are sent to the output stream. Each pair of hash partitions is compared...

22/3,K/17 (Item 8 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

00113876 80-07768

An On-Line Character Recognizer

Simmons, Robert M.

Interface Age v5n3 PP: 110-114 Mar 1980

ISSN: 0147-2992 JRNL CODE: INA

...ABSTRACT: recognizer, allowing input of a symbol constructed from a number of points on the tablet to be **matched** to its corresponding alphanumeric character. Desirable characteristics of a character recognizer include: 1. quick response for interactive...

... of the computer's resources. The algorithm consists of the following modules: 1. a routine to accept **data** from the tablet, 2. a feature **extraction** routine which distinguishes one character from all others, 3. a **table lookup** routine to find a **match** for the input character, and 4. a training routine allowing a user to build a table of characters **matching** his own printing style.

22/3,K/18 (Item 9 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2003 ProQuest Info&Learning. All rts. reserv.

00049760 77-02078

FROM COBOL TO MARK IV

FLYNN, JIM; KIMBER, DICK

DATAMATION V23 N1 PP: 111-120 JAN. 1977

ISSN: 0011-6963 JRNL CODE: DAT

...ABSTRACT: PROBLEMS. IN THE CASE OF MC CULLOCH PROPERTIES INC., ALL EXISTING SYSTEMS SHARED THE LIMITATIONS OF INFLEXIBLE **FILE** STRUCTURE, LENGTHY AND COMPLEX PROGRAMS, AND TIME CONSUMING MAINTENANCE. AS OTHER CHARACTERISTICS EVOLVED THE CHOICE BECAME CLEAR - CONTINUE MAINTAINING OBSOLETE SYSTEMS OR DEVELOP **NEW** ONES. MC CULLOCH QUESTIONED THE USE OF COBOL AS THE SHOP'S PRIMARY LANGUAGE AND AFTER CONSIDERABLE...

... THE ABILITY TO BE HARDWARE INDEPENDENT AND IS FLEXIBLE. AUTOMATIC FEATURES SIMPLIFY OPERATIONS SUCH AS SEGMENT MANIPULATION, **FILE** COORDINATION, **TABLE LOOKUP**, TRANSACTION **MATCHING** AND UPDATING, **TEXT** PROCESSING, AND REPORT FORMATTING. SECONDLY, MARK IV IS MODULAR AND CAN

CODE ADDRESS ITSELF. AND FINALLY, ANALYSTS CAN DEVELOP DETAILED SPECIFICATIONS AS THEY CODE. TABLES.

22/3,K/19 (Item 1 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2003 Resp. DB Svcs. All rts. reserv.

2551102 Supplier Number: 02551102 (USE FORMAT 7 OR 9 FOR FULLTEXT)
MMC, Lara team up on net processing
(MMC Networks to offer Lara Technology Inc's SuperCAM search engines with
MMC's family of network processors)
Electronic Engineering Times, p 24
August 16, 1999
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 86

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:

...plans to combine MMC's network processors with Lara's SuperCAM engines-which are based on content- **addressable** memories-into single-chip solutions, Lara's **new** ternary memories will be co-marketed with MMC's network processors to provide **more** efficient **look - up table** architectures for policy-based networking requiring multiple **parallel searches** of Internet Protocol **packet** headers, the companies said.

August 16, 1999

...

22/3,K/20 (Item 2 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2003 Resp. DB Svcs. All rts. reserv.

2550654 Supplier Number: 02550654 (USE FORMAT 7 OR 9 FOR FULLTEXT)
C-Port's massive chip creates buzz, questions -- Network processor totes 17
RISC cores
(C-Port Corp unveils new C-5 digital communications processor as what may
be most highly integrated single-chip offering in the growing market of
network processors)
Electronic Engineering Times, p 1
August 16, 1999
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1224

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:

...conjunction with header processors for such functions as Internet Protocol differentiated services.

Various algorithms

C-Port's **table lookup** unit can be soft-configured for a variety of table algorithms often implemented in CAMs or SRAMs, such as longest-prefix- **match searches** or secure hash algorithms. One TLU can handle multiple lookup algorithms simultaneously, for advanced Layer 3 and ...

...requiring multi-dimensional header analysis. The TLU can handle up to 133 million lookups per second, or **more** than 50 million IPv4 lookups per second, exceeding IPv4 **packet** -stream rates in OC-192 (10-Gbit) channels.

The final two processors on-chip, the queue manager...

22/3,K/21 (Item 3 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2003 Resp. DB Svcs. All rts. reserv.

2521267 Supplier Number: 02521267 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Kawasaki rolls CAM search engine, preps classifier
(Kawasaki LSI USA is introducing GigaCAM content-addressable memories; Lara
Technology is introducing high-density content-addressable memories based
on ternary memory structures)
Electronic Engineering Times, p 38
July 12, 1999
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 566

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
By: Loring Wirbel

San Jose, Calif. - The summer stampede among vendors of content-
addressable memories (CAM) indicates how desperately developers of edge
routers need to reduce memory costs as **lookup tables** for networking
addresses grow **more** varied and complex. Kawasaki LSI USA Inc., one of
the few consistent developers of CAMs since their renaissance in the early
1990s, is sampling a longest- **match search** -engine CAM based on a binary
architecture, and promising fall delivery of a classification engine that
uses a mixed-mode binary/ternary structure to handle a combination of **data**
- **link** , Internet-Protocol and TCP layer search duties.

Kawasaki will have other vendors hot on its heels. Within...

22/3,K/22 (Item 4 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2003 Resp. DB Svcs. All rts. reserv.

2336298 Supplier Number: 02336298 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Routing around the incumbents
(US sales from toll calls are estimated at \$10.9 bil/yr; new firms may have
an advantage over ILECs in local call routing)
America's Network, v 102, n 23, p 28+
December 01, 1998
DOCUMENT TYPE: Journal; Industry Overview ISSN: 1075-5292 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1653

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...calls properly (Figure 2). Most LCR-capable PBXs use complex structures
for defining the routes based on **blocks** of 10 or 100 numbers. A better
method is to use a **more** general mechanism based on pattern **matching** ; as
digits are dialed, they are **matched** against a detect table. When a **match**
is found, the detect table entry points to an output table. The output
table defines the primary...

22/3,K/23 (Item 5 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2003 Resp. DB Svcs. All rts. reserv.

1987173 Supplier Number: 01987173 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Pattern-matching processor could speed net routing
(NeoCore and UTMIC Microelectronic Systems working together to develop new

approaches to high-speed processor design)
Electronic Engineering Times, p 01
November 10, 1997
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1167

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:

...on a distributed system where many associative processors share a common associative memory.

This ability to accelerate **matching** by adding processors may be a powerful **new** tool for breaking open network-routing bottlenecks. Today, a fast processor must read the **address** in a **packet** header and sequentially search through its **routing tables** to find out what to do with the **packet**. In theory, **packet** forwarding for an Internet Protocol router could be speeded from 250,000 **packets** /s-top speed for traditional sequential list **matching** -to 30 million **packets** /s for an associative-processor router.

But Brandin said that design teams at internetworking OEMs are very...

22/3,K/24 (Item 6 from file: 9)
DIALOG(R)File 9:Business & Industry(R)
(c) 2003 Resp. DB Svcs. All rts. reserv.

1907242 Supplier Number: 01907242 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Motorola's Scorpion Chip Turns TVs Into Interactive Sets
(Called the Scorpion chip, the MC92100 from Motorola's Semiconductor Products Sector will provide flexible, television based graphics overlay and mixing)
Newsbytes News Network, p N/A
August 05, 1997
DOCUMENT TYPE: Journal ISSN: 0983-1592 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 503

ABSTRACT:

...audio/video products operation, interactive features will include Internet browsing and an electronic program guide in both **new** and existing Motorola products. Evans said that Scorpion graphics **match** the resolution and color depth of standard NTSC/PAL baseband video. The system also will allow products...

...Committee) formats. The encoder also has closed caption inserter. Scorpion will support a wide range of graphics **data** formats, including YCrCb (4:2:2), RGB16 (565 and 555), as well as 2/4/8 bit Color **Look Up Tables** (CLUT). All formats support alpha mixing/transparency on a pixel or window basis. ...

22/3,K/25 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

04185674 Supplier Number: 54760748 (USE FORMAT 7 FOR FULLTEXT)
Intel Discloses New IA-64 Features; Rotating Registers Reduce Code Expansion; Merced Touted for Big Servers. (microprocessor) (Product Information)
Microprocessor Report, v13, n3, pNA
March 8, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Refereed; Trade
Word Count: 3343

(USE FORMAT 7 FOR FULLTEXT)

TEXT:

...talks at the recent Intel Developers Forum, the company tantalized industry watchers by dribbling out a few **more** details about its IA-64 instruction set and its first implementation, Merced. In a joint presentation by Intel's John Crawford and Hewlett-Packard's Jerry Huck, the two architects shed **additional** light on the IA-64 design. They provided **further** details on the architecture's support for predication and speculation and also described IA-64's branch...

...high-availability features required in large servers. The company asserts that four-processor Merced servers will deliver **more** performance on the TPC-C benchmark than four-way servers using 1-GHz Alpha 21264 processors or...

...can access only the logical registers, the hardware must assign mappings and translate accesses using an associative **lookup table**. This complexity increases die size and often the pipeline depth as well. IA-64 eliminates this hardware complexity with its large register **file** (128 integer, 128 floating-point) that is directly accessible by software. Specifying the physical register names in...

...reorders instructions to cover the latency of the loads. The reordering naturally overlaps instructions from two or **more** iterations of the loop until enough instructions are found to overcome the latency (or the hardware runs...

...the same registers, but these conflicts are resolved by hardware register renaming. An IA-64 processor can **address** the latency problem by unrolling the loop in software. This common compiler technique duplicates the loop instructions...

...expansion, IA-64 uses its rotating registers. With this technique, the upper three-quarters of each register **file** (integer, FP, and predicates) rotates, leaving the lower registers for global variables. Accesses to these upper registers...

...RRBs by one at the end of each loop iteration, allowing the next iteration to use a **new** set of physical registers. (With proper spacing, several variables can be rotated through the register **file** at once.) The rotating predicate registers provide a simple way to handle loop setup (prologue) and termination (branch registers), instead of the integer registers, to hold target **addresses**. These special registers are likely to be physically located near the fetch unit, not the ALUs, and...

...is only one LC register. IA-64 branches include at least two bits to give the compiler **more** control over branch prediction. Like many RISC architectures, IA-64 provides a "hint" as to whether a...

...indicates that software prediction should be used; the hardware predictor can ignore these branches, freeing entries for **more** difficult branches. (The hardware may enter static taken branches into its target-**address** predictor.) This combination of software and hardware prediction should provide **more** accuracy than today's hardware-only branch predictors. Like PA-RISC, IA-64 can combine a comparison...

...instruction must be at the end of a parallel-instruction group. As a special case, two or **more** branches can be placed together at the end of a group to form a multiway branch. All...

...and determine which, if any, branch should be taken. This construction is useful when several short code **blocks** have been combined using predication; all the exit cases can be processed at once. Flexible Design Allows Massive Speculation The recent disclosures indicate that IA-64's predication and speculation capabilities are **more** extensive than previously indicated (see MPR 10/27/97, p. 1). Speculation is used to hoist loads above branches, giving the compiler **more** flexibility to reorganize

code. To handle exceptions, each IA-64 register is tagged with an associated NaT...

...take advantage of the target register (which is undefined when NaT is true) to store the load **address** ; thus, the fixup code must have access to any registers needed to recreate the load **address** . The NaT mechanism allows instructions that use speculatively loaded **data** to be hoisted as well. Any computation instruction sets the target register's NaT bit if any ...

...CHK.S. Note that the recovery code must also redo any speculative calculations after reloading the correct **data** . HP's Huck estimates that half of the instructions in a typical program are likely to execute...

...compiler can do this only if it can guarantee that the load and store use different physical **addresses** . With indirect **addressing** , however, this pointer disambiguation can be impossible at compile time. Reordering processors handle this task easily, since loads and stores are reordered at runtime, after **addresses** have been calculated. To hoist a load above a store, IA-64 uses the LD.A (advanced load) instruction. In addition to performing a normal load, this instruction inserts the load **address** into the ALAT (advanced load **address** table). Subsequent store **addresses** are associatively checked against the ALAT; if a **match** is found, the offending entry is removed. Before using the **data** from an LD.A instruction, an LD.C is needed to see if the entry associated with...

...LD.A. The size of the ALAT is implementation dependent. If an LD.A bumps a "live" **address** from the ALAT, the LD.C (or CHK.A) will reload the **data** , causing a performance loss but no error. Similar structures, such as the P6's MOB (memory reorder...needed by these expensive systems. For example, all of the caches and system buses are protected from **data** loss using ECC or other techniques. Corrupted **data** is corrected when possible; if not, it can be marked as bad and the affected process terminated...

...out failed DRAMs. It handles up to four Merced processors and can be used as a building **block** in larger systems, although several Intel customers are developing their own system logic to connect eight or **more** Merced processors. The 460GX supports hot plugging on up to four PCI buses, each at up to 64 bits and 66 MHz for **extra** bandwidth. The multichip set can also be used in workstations, as it includes an AGP 4[en...

...lid, reducing heat density. The system maker must attach a large heat sink to the module to **further** dissipate the heat. Intel has not disclosed the power of the processor, but the package design clearly implies that it will be high; we estimate the Merced module will dissipate **more** than 70 W. Merced Nearing Tapeout The Merced design team has made much progress since the major...

...is ready for system shipments. This schedule seems somewhat aggressive for a high-end processor implementing a **new** instruction set and aimed exclusively at multiprocessor-capable systems; we would not be surprised if system shipments...

...for McKinley will support legacy memory and I/O from the 460GX. McKinley will also use no **more** power or board space than Merced, avoiding chassis redesign. IA-64 Performance Debate Unsettled The **new** details of IA-64 highlight its philosophy of moving complexity from the hardware to the compiler. With these **new** features, an IA-64 compiler can perform most of the code motions handled by hardware in a...

...across an arbitrarily large group of instructions, whereas reordering hardware is limited to a window of no **more** than 80 instructions in today's implementations. Without predication and access to large register **files** , RISC compilers cannot perform the same optimizations and must rely on the hardware. Initial criticisms of ...scheduling, which ignores dynamic information available to the hardware at runtime. Some of the newly disclosed features **address** these issues and show how IA-64 combines static and dynamic scheduling. The ALAT, for example, allows...

...is that dynamic features add hardware complexity. Initially, it appeared that an IA-64 design might be **more** compact than an out-of-order processor by eliminating the instruction-reordering and register-renaming logic. IA ...

...their RISC counterparts, when combined with other IA-64 features such as predication and the large register **files**, they are likely to limit any die-size advantage IA-64 might have over RISC. Code size...

...although these infrequently executed routines aren't likely to do much, other than take up disk space. **More** critical are the aligned branch targets and the 41-bit instructions themselves, which are 33% larger than RISC instructions. An increase in code size reduces the effectiveness of the instruction cache and requires **more** bandwidth from the system bus and from main memory. The large register **file** improves performance by reducing **data**-cache accesses, but it creates a problem on context switches. Saving state requires storing 128 integer registers...

...20-30%, significant but not impossible for competitors to overcome. If Intel delivers strong implementations, they should **match** or exceed the performance of the fastest competitive chips. Merced may not be the best implementation of...

...both system and software vendors is strong and unwavering. As we have seen with x86, this support, **more** than any technical merits or demerits, determines the fate of a **new** microprocessor.

22/3,K/26 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

03873657 Supplier Number: 48458225 (USE FORMAT 7 FOR FULLTEXT)
-CAPS LOGISTICS: CAPS Logistics introduces vehicle routing suite of
products
M2 Presswire, pN/A
May 1, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 719

(USE FORMAT 7 FOR FULLTEXT)
TEXT:

...290498 CAPS Logistics, Inc., the premier vendor of software for optimizing logistics planning and scheduling, announces a **new** integrated suite of vehicle routing and scheduling products. The suite includes the **new** Version 6.0 of RoutePro Dispatcher for operational vehicle routing and three **new** products: RoutePro Designer for strategic route optimization and analysis, RoutePro Residential for residential route optimization, and RoutePro...

...the effect of strategy changes on dispatch operations before actual implementation. RoutePro Dispatcher allows users to build **new** routes from scratch or adapt daily customer order fluctuations to current master routes. Then, users can dispatch...

...route planning. Built on top of RoutePro Designer, RoutePro Residential includes the industry's leading mapping and **address matching** technologies to optimize routes that must cover a large number of customers in concentrated areas (e.g...

...interactive map-based graphics through a Windows NT/95 interface to assist users in understanding and changing **routing** strategies. These **graphics** illustrate territory workloads and underutilized routes. Extensive drag and drop capabilities allow users to easily edit territory ...

...CAPS Logistics has the best routing package commercially available," said Larry Sur, President of Schneider Logistics, Inc. New routing clients signed this quarter include Imperial Oil Limited, AMR Global Logistics, Rollins Logistics, Rollins, Inc., Fresh...

...product, the CAPS Logistics Toolkit, a modeling workbench for building custom supply chain decision support solutions. With more than 1,100 product installations in 22 countries worldwide, CAPS Logistics has grown 500% over the last...

...e-mail: marilyn.kapaun@caps.com *M2 COMMUNICATIONS DISCLAIMS ALL LIABILITY FOR INFORMATION PROVIDED WITHIN M2 PRESSWIRE. DATA SUPPLIED BY NAMED PARTY/PARTIES.*

22/3,K/27 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

03139751 Supplier Number: 46429114 (USE FORMAT 7 FOR FULLTEXT)

Rainbow

Prepress Commentary, v2, n1, pN/A

June 1, 1996

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 1264

... about 50% of their analogue equivalent.

Version 4.2 of the Rainbow software is now optimised for more RAM power, and includes colour target calibration and look - up tables (LUTs) for colour adjustment values and maintaining ink ribbon consistency through bidirectional calibration. Also included are the...

...of RGB direct proofing for digital photography, and Pantone libraries. It is now possible to save Ripped files and to purchase the optional Euro colour calibration software module. This makes it possible to copy a...

...100%, due to the number of variables, Imation has introduced Rainbow Colour Locking. This is a consistency control system that matches proofs to a press so that remote proofing is more reliable. It takes about 15 minutes with a spectrophotometer to measure and then lock proofing parameters for proof to proof consistency. This is also an optional extra, and, like the calibration module, costs around \$2000 in the UK.

Currently 43% of 3M's proofing...

22/3,K/28 (Item 4 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2003 The Gale Group. All rts. reserv.

01079561 Supplier Number: 40692084 (USE FORMAT 7 FOR FULLTEXT)

IBM ANNOUNCEMENTS

Computergram International, n1123, pN/A

Feb 24, 1989

Language: English Record Type: Fulltext

Document Type: Newswire; Trade

Word Count: 1147

IBM's second stab at new product announcements late on Tuesday -which caught the UK on the hop, because none of the late...

...in its February 21 bulletin. As well as the three highlights on yesterday's front page - the new 3092 controllers, big price cuts on AS/400 and 9370 memory, and special offer on 3270s traded...

...from the workstation to a host CICS system using SNA Logical Unit 6.2 protocols. Under the new Transaction Routing from the Workstation

feature, when the thing is running under OS/2 Extended Edition, CICS...

...and executed as if it had been entered from a 3270 terminal attached to the host. The **routing** is **table** controlled, is not dependent on the application program, and it is transparent to the user. Transaction routing ...

...particularly useful for application migration. And users can invoke host transactions accessing host DB2 or DL/I **data**, with the results returned to the PS/2. Support for 3270 extended datastreams is as currently provided ...

...Support. Transaction routing and function shipping is from the workstation to the host only. Shippable terminal functions, **message** protection, and functions such as paging are not supported. The bad news - perhaps - is that there are...

...OS/2 transactions provided by IBM, but if you start trying to be clever, you may need **more** space still for some applications. Users will also need either a Micro Channel PS/2 with 3270...

...processor, prior to download to and installation on the micro, the host needs any supported tape device **matching** the density of the distribution tape (figures!), and 10Mb of disk storage for CICS OS/2. On...

...And to download CICS OS/2 from a host to a micro, users need IBM 3270-PC **File** Transfer program 1.1.1 for an MVS host; for DOS/VSE, a **file** transfer capability is included within VSE/SP 2.1.4 and later, but other **file** transfer programs can be used. CICS OS/2 is \$675 for the first, \$575 for subsequent copies...

22/3,K/29 (Item 1 from file: 813)
DIALOG(R) File 813:PR Newswire
(c) 1999 PR Newswire Association Inc. All rts. reserv.

1197471 NYTU132
**Optus Software Extends Functionality of the HP Network ScanJet 5 with
FACSys Fax Server Integration**

DATE: December 9, 1997 14:58 EST WORD COUNT: 786

...digital document image.

Users will also be able to take advantage of FACSys' inbound routing capabilities to **more** easily direct **documents** scanned at the Network ScanJet 5 to their own desktops. When users enter their ID, the network scanner **looks** up the **corresponding** entry in the FACSys **routing look
- up table** and routes the **document** accordingly.

"We're taking the principle behind faxing -- which is the routing of a scanned document -- and...

22/3,K/30 (Item 1 from file: 16)
DIALOG(R) File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

06659166 Supplier Number: 55851851 (USE FORMAT 7 FOR FULLTEXT)
**Excel's Third Lookup Choice: Match : A more versatile lookup function can
be an invaluable tool for getting the information you need.**
Stinson, Craig
PC Magazine, p183
Oct 19, 1999
Language: English Record Type: Fulltext Abstract
Document Type: Magazine/Journal; General Trade
Word Count: 982

... pluck some particular value from a list or table that wasn't originally designed to be a **lookup table** ? For that need, Excel supplies a third lookup function, called **match** . **More** versatile than vlookup and hlookup, **match** in conjunction with other functions ;can be an invaluable tool for getting the information you need out of your spreadsheet **data** . We'll look at several applications for **match** here.

Minimum Daily Balance

The first problem involves a cash-flow application. Deposits, checks, miscellaneous bank transactions...

22/3,K/31 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

06565123 Supplier Number: 55459281 (USE FORMAT 7 FOR FULLTEXT)
C-Port's massive chip creates buzz, questions -- Network processor totes 17 RISC cores. (Product Announcement)
Wirbel, Loring
Electronic Engineering Times, p1
August 16, 1999
Language: English Record Type: Fulltext
Article Type: Product Announcement
Document Type: Magazine/Journal; Trade
Word Count: 1236

... conjunction with header processors for such functions as Internet Protocol differentiated services.

Various algorithms

C-Port's **table lookup** unit can be soft-configured for a variety of table algorithms often implemented in CAMs or SRAMs, such as longest-prefix- **match searches** or secure hash algorithms. One TLU can handle multiple lookup algorithms simultaneously, for advanced Layer 3 and ...

...requiring multi-dimensional header analysis. The TLU can handle up to 133 million lookups per second, or **more** than 50 million IPv4 lookups per second, exceeding IPv4 **packet** -stream rates in OC-192 (10-Gbit) channels.

The final two processors on-chip, the queue manager...

22/3,K/32 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

06481348 Supplier Number: 55130547 (USE FORMAT 7 FOR FULLTEXT)
Kawasaki rolls CAM search engine, preps classifier. (Kawasaki LSI USA's content-addressable memory technology) (Company Business and Marketing)
Wirbel, Loring
Electronic Engineering Times, p38
July 12, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 570

(USE FORMAT 7 FOR FULLTEXT)

TEXT:

...indicates how desperately developers of edge routers need to reduce memory costs as lookup tables for networking **addresses** grow **more** varied and complex. Kawasaki LSI USA Inc., one of the few consistent developers of CAMs since their renaissance in the early 1990s, is sampling a longest-**match search** -engine CAM based on a binary architecture, and promising fall delivery of a classification engine that uses a mixed-mode binary/ternary structure to handle a combination of **data - link** , Internet-Protocol and TCP layer search duties.

22/3,K/33 (Item 4 from file: 16)
DIALOG(R) File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

05834264 Supplier Number: 50345496 (USE FORMAT 7 FOR FULLTEXT)

Shining Up Your Data

Craig, Robert

ENT, v3, n16, p50

Oct 7, 1998

Language: English Record Type: Fulltext

Article Type: Article

Document Type: Magazine/Journal; Professional

Word Count: 734

Application programmers usually deal with **data** quality by implementing edit tests at **data** entry fields. For example, a series of tests for a name will be first, to find out...

...partner, supplier, patient, whatever) is known to the system. If it is, or if there is a **match** with a number of potential candidates, the programmer presents the user with a pick list, with perhaps a default choice. A **match** may be found using a simple **table** of database **lookup**, a Soundex search, or some other, **more** sophisticated, mechanism.

If, on the other hand, the system doesn't find a potential match, the program...

22/3,K/34 (Item 5 from file: 16)
DIALOG(R) File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

05400780 Supplier Number: 54470970 (USE FORMAT 7 FOR FULLTEXT)

The digital diet.

Wright, Guy

Interactivity, v3, n4, p21(1)

April, 1997

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 7507

... PCX.

Two variations on the RLE approach are LZW (Lempel-Ziv-Welch), found in GIF and TIFF **file** formats, and Huffman encoding. (A variation on Huffman, CCITT, is commonly used for fax transmissions.) These methods analyze a **file** for redundancies or patterns and generate a **lookup table** of patterns. GIF uses a predetermined fixed-length table representing colors. TIFF uses variable-length tables. (When a table is filled, it can be discarded and a **new** one built on the fly.) Huffman encoding assigns low numbers to patterns that occur most frequently and...

...frequent patterns. Then it generates a list of code numbers that point to the patterns in the **lookup table**. Even though rare or unique patterns may require **more** bytes, fewer bytes are required to send the majority of the information. With GIF **files** and fax machines, the **lookup tables** are predetermined. The color table for GIF is always the same, so it's up to the display application to **match** codes to colors. Tables that are supposed to work well on typical business **documents** are permanently stored in every fax machine's ROM. When you send a fax, only the pattern codes are sent. In cases where a unique **lookup table** is generated based on a particular **file**, the pattern table has to be sent along with the codes.

You can think of a computer...

22/3,K/35 (Item 6 from file: 16)
DIALOG(R) File 16:Gale Group PROMT(R)

(c) 2003 The Gale Group. All rights reserved.

05332180 Supplier Number: 48114249 (USE FORMAT 7 FOR FULLTEXT)

Pattern-matching processor could speed net routing

Wirbel, Loring

Electronic Engineering Times, p1

Nov 10, 1997

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 1174

... on a distributed system where many associative processors share a common associative memory.

This ability to accelerate **matching** by adding processors may be a powerful **new** tool for breaking open network-routing bottlenecks. Today, a fast processor must read the **address** in a **packet** header and sequentially search through its **routing tables** to find out what to do with the **packet**. In theory, **packet** forwarding for an Internet Protocol router could be speeded from 250,000 **packets /s** to top speed for traditional sequential list **matching** - to 30 million **packets /s** for an associative-processor router.

But Brandin said that design teams at internetworking OEMs are very...

22/3,K/36 (Item 7 from file: 16)

DIALOG(R)File 16:Gale Group PROMT(R)

(c) 2003 The Gale Group. All rights reserved.

05102225 Supplier Number: 47490593 (USE FORMAT 7 FOR FULLTEXT)

Meeting of minds

Fisher, David

Electronics Times, p34

June 26, 1997

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 1550

... overcome by re-architecture, 'doing more of the logical operations in parallel'.

Foss recommends going a stage **further** and moving logic functions into the memory **blocks** themselves, using a combination of **additional** registers for **look - up tables** and logic which is pitch- **matched** to the columns.

Finally, there is the problem of testing. Embedded behind a processor or dedicated logic...

22/3,K/37 (Item 8 from file: 16)

DIALOG(R)File 16:Gale Group PROMT(R)

(c) 2003 The Gale Group. All rights reserved.

04712415 Supplier Number: 46938546 (USE FORMAT 7 FOR FULLTEXT)

MULT-LINK CELEBRATING TEN YEARS OF PRODUCT AND CUSTOMER SERVICE EXCELLENCE,

Will introduce new product during consumer electronics show in January

News Release, pN/A

Dec 2, 1996

Language: English Record Type: Fulltext

Document Type: Magazine/Journal; Trade

Word Count: 798

(USE FORMAT 7 FOR FULLTEXT)

TEXT:

New Product, EL CID, Creates Communications Management System to Capture Small Office/Home Office Sales Lexington, Ky, December 2, 1996 - Multi-**Link**, Inc. announced today that it will introduce EL CID, the communications management system that processes, routes and **blocks** calls automatically based on Caller ID, touch tones and fax (CNG) protocol, at

the Consumer Electronics Show...

...true plug and go installation, EL CID targets the growing Small Office/Home Office (SOHO) market. Multi- **Link** plans to ship EL CID product in the first quarter, 1997. The EL CID announcement comes as Multi- **Link** celebrates its tenth year of operation. EL CID gives users the ability to predetermine the routing and processing of incoming voice, **data** and fax calls throughout a small office or home. Using Caller ID information sent over analog phone...

...nearly 50 million home offices in the United States, the home phone line of today handles much **more** than personal calls," says John Stotz, marketing manager at Multi- **Link** . "EL CID provides a cost-effective method to disperse incoming calls to specific phones or equipment throughout...

...savings and information are the driving forces behind EL CID," says Wayne Mulberry, general manager at Multi- **Link** . "With EL CID, Multi- **Link** offers the SOHO market advanced call management capabilities in a product that pays for itself in phone...

...featured "line sharing" capabilities for automatic detection and routing of fax and modem calls, similar to Multi- **Link** 's award-winning call processor, The Stick. Through the RS-232 serial port, EL CID sends Caller ID information to the software program where the system **matches** information with entries in call **routing tables** established by the user. The program then tells EL CID to grab the line, and to route calls to controller ports and/or module locations, or to ring nothing (call **block**). EL CID can remove itself from specific incoming calls to ring extension phones not connected to EL...

...For the user who hates to leave the PC on constantly, EL CID can download a call **routing table** into the control unit for "after hours" operation. With a user-friendly software interface and plug and go installation, Multi- **Link** will make EL CID available through a variety of selling channels, including telephony and computer equipment dealers...

...CID is ideal for resellers that reach the SOHO market," says Phillip Lovin, sales manager at Multi- **Link** . "installation is as simple as plugging in a phone and connecting a serial cable." Multi- **Link** , Inc., headquartered in Nicholasville, Ky., is a leading supplier of communications management products for business, small office...

...processor, The Stick, is used by Fortune 500 companies, small businesses and homes throughout the world. Multi- **Link** 's remote power controller, The Power Stone, provides power control, reboot and power status for off-site computers and equipment over a standard phone line. Multi- **Link** was founded in 1987.

22/3,K/38 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)
(c) 1999 The Gale Group. All rts. reserv.

01518236

Imaging Technology Incorporated Introduces Software Library for its Series 151 Product Line.

NEWS RELEASE September 2, 1986 p. 11

... supplier of image processing hardware and software to the OEM marketplace, today announced the availability of a **new** software package for its faster- than-real-time Series 151 product line. ITEX 151 (TM) is a ...

... for use with Imaging Technology's Series 151 Image Processor, ITEX 151 includes: board-level access and **control** routines **look - up table** operations image filtering and convolutions -- edge-detection, sharpening graphics image geometry -- rotate, mirror, zoom image processing and

statistical analysis -- subtraction, averaging, histogram. ITEX 151 is distributed as **object** code on a high-density, MS/DOS-compatible floppy disk. Routines are callable from high-level programming languages, including Microsoft C and Computer Innovations, Inc. C. Extensive **documentation** is also included. ...

Sec	Items	Description
S1	2460702	(IP OR INTERNET() PROTOCOL OR NETWORK) () ADDRESS OR URL OR U- RLS OR (UNIFORM OR UNIVERSAL) () RESOURCE() LOCATOR? OR ADDRESS? OR LINK? ? OR NAMESPACE? OR DOMAIN?
S2	26506	(HASH OR LOOKUP OR LOOK() UP OR ROUTING OR PREFIX OR MASK) - (2N) (TUPLE OR TABLE? OR ARRAY? OR (MATHEMATICAL OR DATA) () EL- EMENT? OR MATRIX? OR MATRICES OR COLUMN? OR ROW? OR GRAPH?) OR DHT
S3	677383	(PARALLEL? OR MATCH? OR EQUAL? OR CORRESPOND? OR CONTROL? - OR PARITY OR ALIGNMENT) (2N) (SEARCH? OR QUEST? OR PURSU? OR SE- EK? OR QUER? OR MATCH? OR FIND? OR LOOK? ? OR LOOKING)
S4	11048045	DOCUMENT? OR FILE? OR OBJECT? OR PACKET? OR BLOCK? OR DATA OR MESSAGE OR E-MAIL OR EMAIL OR TEXT
S5	153845	(SECONDARY OR FURTHER OR ADDITIONAL OR NEW OR SUPPLEMENT? - OR MORE OR EXTRA?) (2N) (TUPLE OR TABLE? OR ARRAY? OR (MATHEMA- TICAL OR DATA) () ELEMENT? OR MATRIX? OR MATRICES OR COLUMN? OR ROW? OR GRAPH?)
S6	1193	(MULTIPL? OR MANY OR PLURAL? OR NUMEROUS OR SEVERAL OR DUP- PLICATE OR UNLIMITED) (2W) S5
S7	329	S1 AND S2 AND S3
S8	0	S7 AND S6
S9	7	S7 AND S5
S10	1473	S2 AND S3
S11	0	S10 AND S6
S12	887	S10 AND S4
S13	261	S12 AND S1
S14	5	S13 AND S5
S15	7	S9 OR S14
S16	4	S15 NOT PY>1999
S17	261	S7 AND S4
S18	118	S17 AND (SECONDARY OR FURTHER OR ADDITIONAL OR NEW OR SUPP- LEMENT? OR MORE OR EXTRA?)
S19	113	S18 NOT S15
S20	79	S19 NOT PY>1999
S21	79	S20 NOT PD>19991213
S22	58	RD (unique items)
File	35:	Dissertation Abs Online 1861-2003/Sep (c) 2003 ProQuest Info&Learning
File	8:	Ei Compendex(R) 1970-2003/Oct W4 (c) 2003 Elsevier Eng. Info. Inc.
File	103:	Energy SciTec 1974-2003/Oct B2 (c) 2003 Contains copyrighted material
File	2:	INSPEC 1969-2003/Oct W4 (c) 2003 Institution of Electrical Engineers
File	202:	Info. Sci. & Tech. Abs. 1966-2003/Sep 16 (c) 2003 EBSCO Publishing
File	65:	Inside Conferences 1993-2003/Nov W1 (c) 2003 BLDSC all rts.reserv.
File	233:	Internet & Personal Comp. Abs. 1981-2003/Jul (c) 2003, EBSCO Pub.
File	94:	JICST-EPlus 1985-2003/Nov W1 (c) 2003 Japan Science and Tech Corp(JST)
File	239:	Mathsci 1940-2003/Dec (c) 2003 American Mathematical Society
File	6:	NTIS 1964-2003/Nov W1 (c) 2003 NTIS, Intl Cpyrgh All Rights Res
File	144:	Pascal 1973-2003/Oct W4 (c) 2003 INIST/CNRS
File	434:	SciSearch(R) Cited Ref Sci 1974-1989/Dec (c) 1998 Inst for Sci Info
File	34:	SciSearch(R) Cited Ref Sci 1990-2003/Oct W4 (c) 2003 Inst for Sci Info
File	95:	TEME-Technology & Management 1989-2003/Oct W3 (c) 2003 FIZ TECHNIK
File	99:	Wilson Appl. Sci & Tech Abs 1983-2003/Sep (c) 2003 The HW Wilson Co.
File	241:	Elec. Power DB 1972-1999Jan

16/5/1 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6450333 INSPEC Abstract Number: B2000-02-6210L-060, C2000-02-6150N-044

Title: Hash parallel and label parallel routing for high performance multicast router with fine grain QoS control

Author(s): Ohta, M.; Sola, M.; Fujikawa, K.; Kojima, A.; Fukumori, H.; Muraoka, Y.

Author Affiliation: Tokyo Inst. of Technol., Japan

Conference Title: 1999 Internet Workshop. IWS99. (Cat. No.99EX385) p. 13-16

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 **Country of Publication:** USA ix+302 pp.

ISBN: 0 7803 5925 9 **Material Identity Number:** XX-1999-00826

U.S. Copyright Clearance Center Code: 0 7803 5925 9/99/\$10.00

Conference Title: Proceedings of 1999 Internet Workshop (WS'99)

Conference Sponsor: Project entitled 'Integrated Network Archit. Adv. Multimedia Application Syst.' Japan Soc. Promotion of Sci. (JSPS) (JSPS-RFTF97R16301); Sci. & Technol. Agency 'Int. workshop on adv. multimedia commun. network in Asia-Pacific area'; IEEE Commun. Soc.; Asia-Pacific Adv. Network (APAN); Commun. Res. Lab. (CRL), MPT; Comput. Center, Osaka Univ.; Internet Res. Committee (IRC) of IEICE of Japan; Internet Technol. Res. Committee (TRC) of JSPS; High Quality Internet (HQI) Study Group of Inf. Process. Soc. Japan (IPSJ) WIDE Project

Conference Date: 18-20 Feb. 1999 **Conference Location:** Osaka, Japan

Language: English **Document Type:** Conference Paper (PA)

Treatment: Practical (P)

Abstract: **Routing table lookup**, or its memory latency, is the most serious bottleneck of high performance routing. Flow-wise or group-wise **routing table** entries for QoS guaranteed or multicast communications need a large **routing table**, which further increase the latency. Recent routers have multiple input interfaces and output interfaces connected by a high bandwidth cross connect. Such architecture allows **parallel routing table look up** at each interface but the number of interfaces limits the parallelism. By having two cross connects, one between input interfaces and routing engines, the other between the routing engines and output interfaces, it is possible to make the **routing table look up** unlimitedly **parallel**. The remaining problem is how to decide the proper routing engine at the input interface. Hash parallel routing is a technique to use the hashed value of the destination **addresses** of **packets** to decide the routing engine. Label parallel routing is a technique to decide the routing engine at the time of signaling and ask the router at the previous hop to put the decision result in the **link label**.

(4 Refs)

Subfile: B C

Descriptors: **file** organisation; internetworking; multicast communication; parallel programming; quality of service; **table lookup**

Identifiers: label parallel routing; hash parallel routing; high performance multicast router; fine grain QoS control; **routing table lookup**; memory latency; high performance routing; group-wise **routing table** entries; QoS guaranteed communications; multicast communications; large **routing table**; multiple input interfaces; output interfaces; high bandwidth cross connect; **parallel routing table look up**; cross connects; input interfaces; routing engines; routing engine

Class Codes: B6210L (Computer communications); B6150 (Communication system theory); C6150N (Distributed systems software); C6110P (Parallel programming); C6130 (Data handling techniques); C6120 (File organisation)

Copyright 1999, IEE

16/5/2 (Item 2 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

4829106 INSPEC Abstract Number: B9501-6140C-086, C9501-1250-035

Title: New developments on geometric hashing for curve matching

Author(s): Gueziec, A.; Aya, N.
Author Affiliation: INRIA, Sophia-Antipolis, France
p.703-4
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1993 Country of Publication: USA xviii+804 pp.
ISBN: 0 8186 3880 X
U.S. Copyright Clearance Center Code: 1063-6919/93/\$03.00
Conference Title: Proceedings of IEEE Conference on Computer Vision and
Pattern Recognition
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Pattern Anal. &
Mach. Intelligence
Conference Date: 15-17 June 1993 Conference Location: New York, NY,
USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)

Abstract: The problem of fast rigid **matching** of 3D curves with subvoxel
precision is **addressed**. More invariant parameters are used, and **new**
hash tables are implemented in order to process larger and more complex
sets of **data** curves. There exists a Bayesian theory of geometric hashing
that explains why local minima are not really a problem. The more likely
transformation always wins. It is also possible to predict the uncertainty
on the **match** with the help of the Kalman filter, and compare it with real
measures. (4 Refs)

Subfile: B C

Descriptors: Bayes methods; differential geometry; **file** organisation;
image **matching**; invariance; Kalman filters; splines (mathematics)

Identifiers: geometric hashing; curve **matching**; fast rigid **matching**;
3D curves; subvoxel precision; **hash tables**; **data** curves; Bayesian
theory; local minima; uncertainty; Kalman filter

Class Codes: B6140C (Optical information, image and video signal
processing); B0240Z (Other topics in statistics); B0250 (Combinatorial
mathematics); B0290F (Interpolation and function approximation); C1250 ((Pattern recognition); C1140Z (Other topics in statistics); C1160 (Combinatorial mathematics); C6120 (File organisation); C4130 (Interpolation and function approximation); C1260 (Information theory)

16/5/3 (Item 3 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

02760318 INSPEC Abstract Number: A86117056, B86063876, C86055883

Title: Truth- table look - up parallel data **processing using an**
optical content- addressable memory

Author(s): Mirsalehi, M.M.; Gaylord, T.K.

Author Affiliation: Sch. of Electr. Eng., Georgia Inst. of Technol.,
Atlanta, GA, USA

Journal: Applied Optics vol.25, no.14 p.2277-83

Publication Date: 15 July 1986 Country of Publication: USA

CODEN: APOPAI ISSN: 0003-6935

U.S. Copyright Clearance Center Code: 0003-6935/86/142277-07\$02.00/0

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: The extension of truth- table look - up processing beyond
primitive operations (such as addition) to higher-level operation (such as
discrete **matched** filtering) is presented. Use of the residue system and
logical minimization techniques to reduce the required number of reference
patterns stored in a content- **addressable** memory is illustrated for 16-bit
full-precision addition. Multilevel coding of the numbers is introduced as
a method to achieve **further** truth- table reduction. The required number
of reference patterns for implementing the residue addition and
multiplication operations are provided for all moduli from 2 through 32
with 2-, 3-, and 5-level coding. An optical holographic implementation of a
system that processes multilevel coded numbers is presented. (14 Refs)

Subfile: A B C

Descriptors: holography; optical information processing; optical storage;
table lookup

Identifiers: multilevel number coding; parallel data processing;
optical content- addressable memory; truth- table look - up processing;
primitive operations; addition; higher-level operation; discrete matched
filtering; residue system; logical minimization techniques; reference
patterns; optical holographic implementation

Class Codes: A4230 (Optical information, image formation and analysis);
A4230N (Optical storage and retrieval); A4240M (Applications); B4350 (Holography); C5270 (Optical computing techniques); C5320K (Optical storage)

16/5/4 (Item 1 from file: 144)
DIALOG(R) File 144:Pascal
(c) 2003 INIST/CNRS. All rts. reserv.

12320786 PASCAL No.: 95-0559819

Highly parallel DSP architecture for image recognition

KAWAI H; INOUE Y; STREITENBERGER R; YOSHIMOTO M

Mitsubishi Electric Corp, Itami-shi, Japan

Journal: IEICE Transactions on Fundamentals of Electronics,
Communications and Computer Sciences, 1995, v E78-A (8) 963-970
ISSN: 0916-8508 CODEN: IFESEX Availability: E.i.

No. of Refs.: 9 Refs.

Document Type: P (Serial) ; A (Analytic)

Country of Publication: Japan

Language: English

This paper presents a newly developed architecture for a highly parallel DSP suited for realtime image recognition. The programmable DSP was designed for a variety of image recognition systems, such as computer vision systems, character recognition systems and others. The DSP consists of functional units suited for image recognition: a SIMD processing core, a hierarchical bus, an Address Generation Unit, Data Memories, a DMA controller, a Link Unit, and a Control Unit. The high performance of 3.2GOPS is realized by the eight-parallel SIMD core with a optimized pipeline structure for image recognition algorithms. The DSP supports flexible data transfers including an extraction of local images from raster scanned image data, a table-loop-up, a data -broadcasting, and a data -shifting among processing units in the SIMD core, for effective execution of various image processing algorithms. Hence, the DSP can process a 5 x 5 spatial filtering for 512 x 512 images within 13.1 msec. Adopting the DSP to a Japanese character recognition system, the speed of 924 characters/sec can be achieved for feature extractions and feature vectors matchings. The DSP can be integrated in a 14.5 x 14.5 mm SUP 2 single-chip, using 0.5 mu m CMOS technology. In this paper, the key features of the architecture and the new techniques enabling efficient operation of the eight parallel processing units are described. Estimation of the performance of the DSP is also presented.

English Descriptors: Image recognition; Hierarchical bus; Address generation unit; Data shifting; Feature vectors matchings ; Application; Parallel processing systems; Computer architecture; Real time systems; Computer vision; Character recognition; Data storage equipment; Hierarchical systems; Computer control systems; Optimization; Algorithms; Table lookup ; Feature extraction ; Image processing; Theory

French Descriptors: Application; Systeme traitement parallele; Architecture ordinateur; Systeme temps reel; Vision ordinateur; Reconnaissance caractere; Equipement stockage donnee; Systeme hierarchise; Systeme commande par ordinateur; Optimisation; Algorithme; Recherche dans table; Detection forme; Traitement image; Theorie

Classification Codes: 001D02B07B; 001D02B; 002A25I; 001D02C; 001D03I02;
001D01A

01751318 ORDER NO: AADAA-IC801152

Enhanced computer performance through adaptive main memory

Author: van Lunteren, Jan

Degree: Dr.

Year: 1998

Corporate Source/Institution: Technische Universiteit Eindhoven (The Netherlands) (0426)

Source: VOLUME 61/01-C OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 301

Descriptors: COMPUTER SCIENCE ; ENGINEERING, ELECTRONICS AND ELECTRICAL

Descriptor Codes: 0984; 0544

ISBN: 90-386-0500-5

Computer performance has improved enormously in the past decade. This is especially due to the large achievements in microprocessor performance which has grown at a rate of 55% per year during this period. In contrast, dynamic random access memory (DRAM) technology, which is the basic building block for the main memory of almost all computer systems, has shown only minor speed improvements. The resulting performance gap, which is widening at an exponential speed, is now threatening to significantly slow down the rate at which computer performance will grow in the near future.

Consequently, main memory performance is soon expected to become the dominant factor in computers, determining overall system performance. From that moment on, putting faster processors into a system will result only in minor speedups. Instead, fundamental gains in computer performance can only be achieved by improving main memory performance.

This thesis presents a revolutionary approach to improve main memory performance. This approach has been inspired by the following two observations concerning conventional main memory designs. The first observation is that, owing to the nature of the techniques that are being applied as a response to the growing performance gap, computer performance is becoming increasingly dependent on how well memory reference properties of programs match the architectural and technological characteristics of the memory system. The second observation is that despite this trend, main memory is characterized by a double transparency. On the one hand, the underlying architecture and technologies are completely transparent to the processor and the programs it executes. On the other hand, main memory only receives individual memory accesses.

The new main memory design presented here aims at eliminating part of these transparencies through the provision of a tighter coupling between software, cache and main memory. This is then used to dynamically adapt main memory operation to the memory reference characteristics of programs and cache controllers.

The design is embedded within the concept of an adaptive main memory, which includes the specification of an adjustable address mapping function, definition of the adaptation targets, a set of adaptation algorithms, models for representing memory access traffic characteristics, and implementation concepts.

Two key elements that have been developed as part of the adaptive main memory concept, and which are unique in their application to main memory design, are a self-similar timing model for memory access traffic and a dynamically adjustable address mapping method based on a lookup table. The presented work has resulted in two patent applications 'Address Mapping for System Memory' [Lunteren97] and 'Address Mapping for Configurable Memory System' [Lunteren98].

The concept has been validated using several memory access traces of well-known benchmark programs. Simulations have demonstrated latency reductions in the range between 25% to 40% for computer and workloads today and in the near future, which correspond to execution speedups between 8% to 38% over conventional main memory designs for single processor systems and between 18% and 43% for multiprocessor systems. (Abstract shortened by UMI.)

22/5/6 (Item 6 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2003 ProQuest Info&Learning. All rts. reserv.

01423684 ORDER NO: AADAA-I9522033

TECHNOLOGY MAPPING OF LOOKUP TABLE BASED FIELD PROGRAMMABLE GATE ARRAYS

Author: DING, YUZHENG

Degree: PH.D.

Year: 1995

Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, LOS ANGELES (0031)

Chair: JASON CONG

Source: VOLUME 56/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 1533. 230 PAGES

Descriptors: COMPUTER SCIENCE; PHYSICS, ELECTRONICS AND ELECTRICITY;
MATHEMATICS

Descriptor Codes: 0984; 0607; 0405

The Field Programmable Gate Array (FPGA) is a very attractive technology for application specific integrated circuit designs due to its advantages of short design cycle and low manufacturing cost for small volume productions. **Lookup - table** (LUT) based FPGAs lead to many applications from circuit emulation to guided missile control due to its reprogrammability. Technology mapping is a crucial step in the FPGA design process and has strong impact on cost and performance. This dissertation **addresses** the technology mapping problems of LUT based FPGAs, with focus on three optimization **objectives**, namely delay minimization, area minimization, and area/delay trade-off.

For delay minimization, we give a strong polynomial time depth-optimal algorithm, and generalize it to a delay-optimal algorithm under arbitrary static net-delay models. These are the first provably optimal polynomial time FPGA mapping algorithms for general K-bounded Boolean networks, representing a theoretical breakthrough. We also propose a scheme for incorporating logic resynthesis into technology mapping, which results in better solution quality with less running time compared with previous approaches. Finally, we show that for dynamic delay models, the delay minimization problem is NP-hard, and propose a heuristic to use dynamic delay information in static delay minimization.

For area minimization, we give an area-optimal duplication-free mapping algorithm that runs in polynomial time. This algorithm is based on our maximum fanout-free cone decomposition of general Boolean networks, which characterizes the network structure and has many other applications. We also give efficient post-processing algorithms for area minimization, which exploit beneficial logic duplication and **matching** based global optimization.

To **further** meet the real design requirements, we propose a scheme for area/delay trade-off in technology mapping. By integrating our area and delay minimization efforts through a set of depth relaxation techniques, for each design we are able to produce a spectrum of solutions with smooth area/delay trade-off, hence offering multiple choices to the designers.

The algorithms have been implemented as a software package and have been thoroughly tested on both benchmark circuits and real designs. Empirical study shows significant improvements over previous algorithms and systems in terms of both delay and area minimization.

22/5/9 (Item 9 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2003 ProQuest Info&Learning. All rts. reserv.

01120399 ORDER NO: AAD90-24254

IMAGE CODING BASED ON ADDRESS VECTOR QUANTIZATION

Author: FENG, YUSHU

Degree: PH.D.

Year: 1990

Corporate Source/Institution: WORCESTER POLYTECHNIC INSTITUTE (0774)
ADVISER: NASSER M. NASRABADI
Source: VOLUME 51/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1981. 180 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL; COMPUTER SCIENCE;
PHYSICS, OPTICS
Descriptor Codes: 0544; 0984; 0752

Image coding is finding increased application in teleconferencing, archiving, and remote sensing. This thesis investigates the potential of Vector Quantization (VQ), a relatively **new** source coding technique, for compression of monochromatic and color images. Extensions of the Vector Quantization technique to the **Address** Vector Quantization method have been investigated. In Vector Quantization, the image **data** to be encoded are first processed to yield a set of vectors. A codeword from the codebook which best **matches** the input image vector is then selected. Compression is achieved by replacing the image vector with the index of the code-word which produced the best **match**, the index is sent to the channel. Reconstruction of the image is done by using a **table lookup** technique, where the label is simply used as an **address** for a table containing the representative vectors. A code-book of representative vectors (codewords) is generated using an iterative clustering algorithm such as K-means, or the generalized Lloyd algorithm.

A review of different Vector Quantization techniques are given in chapter 1. Chapter 2 gives an overview of codebook design methods including the Kohonen neural network to design codebook. During the encoding process, the correlation of the **address** is considered and **Address** Vector Quantization is developed for color image and monochrome image coding. **Address** VQ which includes static and dynamic processes is introduced in chapter 3. In order to overcome the problems in Hierarchical VQ, Multi-layer **Address** Vector Quantization is proposed in chapter 4. This approach gives the same performance as that of the normal VQ scheme but the bit rate is about 1/2 to 1/3 as that of the normal VQ method. In chapter 5, a Dynamic Finite State VQ based on a probability transition matrix to select the best subcodebook to encode the image is developed. In chapter 6, a **new** adaptive vector quantization scheme, suitable for color video coding, called "A Self-Organizing Adaptive VQ Technique" is presented. In addition to chapters 2 through 6 which report on **new** work, this dissertation includes one chapter (chapter 1) and part of chapter 2 which review previous work on VQ and image coding, respectively. Finally, a short discussion of directions for **further** research is presented in conclusion.

22/5/10 (Item 1 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

05763962 E.I. No: EIP01015486204

Title: Routing with a clue

Author: Bremner-Barr, Anat; Afek, Yehuda; Har-Peled, Sarel

Corporate Source: Tel-Aviv Univ, Tel-Aviv, Isr

Conference Title: Proceedings of the 1999 ACM SIGCOMM Conference 'Applications, Technologies, Architectures, and Protocols for Computer Communication'

Conference Location: Cambridge, MA, USA Conference Date: 20990830-20990903

Sponsor: Abrizio; Growth Networks; GTE; MCI Worldcom; et al.

E.I. Conference No.: 56219

Source: Computer Communication Review v 29 n 4 Oct 1999. p 203-213

Publication Year: 1999

CODEN: CCRED2 ISSN: 0146-4833

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 0102W5

Abstract: We suggest a **new** simple forwarding technique to speed-up IP destination **address** lookup. The technique is a natural extension of IP, requires 5 bits in the IP header (IPv4, 7 in IPv6) and performs IP lookup

nearly as fast as IP/Tag-switching but with a smaller memory requirement and a much simpler protocol. The basic idea is that each router adds a 'clue' to each **packet**, telling its downstream router where it ended the IP lookup. Since the forwarding tables of neighboring routers are similar, the clue either directly determines the best prefix **match** for the downstream router, or provides the downstream router with a good point to start its IP lookup. The **new** scheme thus prevents repeated computations and distributes the lookup process across the routers along the **packet** path. Each router starts the lookup computation at the point its up-stream neighbor has finished. Furthermore, the **new** scheme is easily assimilated into heterogeneous IP networks, does not require routers coordination, and requires no setup time. Even a flow of one **packet** enjoys the benefits of the scheme without any **additional** overhead. The speedup we achieve is about 10 times faster than current standard techniques. In a sense this paper shows that the current routers employed in the Internet are clue-less; Namely, it is possible to speedup the IP-lookup by an order of magnitude without any major changes to the existing protocols. (Author abstract) 26 Refs.

Descriptors: Internet; Network protocols; Telecommunication traffic; Congestion control (communication); **Table lookup**; **Packet** switching
Identifiers: Internet protocol (IP)
Classification Codes:
723.1 (Computer Programming)
723 (Computer Software); 716 (Radar, Radio & TV Electronic Equipment);
717 (Electro-Optical Communications); 718 (Telephone & Line Communications)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

22/5/11 (Item 2 from file: 8)
DIALOG(R) File 8:Ei Compendex(R)
(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

05299050 E.I. No: EIP99064697082

Title: Fast IP routing lookup scheme for gigabit switching routers
Author: Huang, Nen-Fu; Zhao, Shi-Ming; Pan, Jen-Yi; Su, Chi-An
Corporate Source: Natl Tsing Hua Univ, Hsin-Chu, Taiwan
Conference Title: Proceedings of the 1999 18th Annual Joint Conference of the IEEE Computer and Communications Societies, INFOCOM-99
Conference Location: New York, NY, USA Conference Date: 19990321-19990325
Sponsor: IEEE Computer Society; IEEE Communications Society
E.I. Conference No.: 55134
Source: Proceedings - IEEE INFOCOM v 3 1999. p 1429-1436
Publication Year: 1999
CODEN: PINFEZ ISSN: 0743-166X
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9908W1

Abstract: One of the key design issues for the **new** generation IP routers is the route lookup mechanism. For each incoming IP **packet**, the IP routing requires to perform a longest prefix **matching** on the **address** lookup in order to determine the **packet**'s next hop. This paper presents a fast route lookup mechanism that only needs tiny SRAM and can be implemented in a pipelined skill in hardware. Based on the proposed scheme, the forwarding table is tiny enough to fit in SRAM with very low cost. For example, a large **routing table** with 40,000 routing entries can be compacted to a forwarding table of 450-470 Kbytes. In the worst case, the number of memory accesses for a lookup is three. When implemented in a pipeline skill in hardware, the proposed mechanism can achieve one routing lookup every memory access. With current 10 ns SRAM, this mechanism furnishes approximately 100 million routing lookups per second. This is much faster than any current commercially available routing lookup schemes. (Author abstract) 13 Refs.

Descriptors: Internet; Network protocols; Routers; **Table lookup**; **Packet** switching; Congestion control (communication); Telecommunication

traffic; **Data** communication systems; Random access storage; storage allocation (computer)

Identifiers: Internet protocol (IP) routing lookup method; Gigabit switching routers

Classification Codes:

723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems)
723 (Computer Software); 716 (Radar, Radio & TV Electronic Equipment);
722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

22/5/12 (Item 3 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

04914068 E.I. No: EIP98014026290

Title: Scalable high speed IP routing lookups

Author: Waldvogel, Marcel; Varghese, George; Turner, Jon; Plattner, Bernhard

Corporate Source: ETH Zurich, Zurich, Switz

Conference Title: Proceedings of the 1997 ACM SIGCOMM Conference on Applications, Technologies, Architectures, and Protocols for Computer Communication

Conference Location: Cannes, Fr Conference Date: 19970914-19970918

E.I. Conference No.: 47675

Source: Computer Communication Review v 27 n 4 Oct 1997. p 25-36

Publication Year: 1997

CODEN: CCRED2 ISSN: 0146-4833

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 9803W3

Abstract: Internet **address** lookup is a challenging problem because of increasing **routing table** sizes, increased traffic, higher speed **links**, and the migration to 128 bit IPv6 **addresses**. IP routing lookup requires computing the best **matching** prefix, for which standard solutions like hashing were believed to be inapplicable. The best existing solution we know of, BSD radix tries, scales badly as IP moves to 128 bit **addresses**. Our paper describes a **new** algorithm for best **matching** prefix using binary search on **hash tables** organized by **prefix** lengths. Our scheme scales very well as **address** and **routing table** sizes increase: independent of the table size, it requires a worst case time of \log_2 (**address** bits) hash lookups. Thus only 5 hash lookups are needed for IPv4 and 7 for IPv6. We also introduce Mutating Binary Search and other optimizations that, for a typical IPv4 backbone router with over 33,000 entries, considerably reduce the average number of hashes to less than 2, of which one hash can be simplified to an indexed array access. We expect similar average case behavior for IPv6. (Author abstract) 19 Refs.

Descriptors: Network protocols; **Data** communication systems; Wide area networks; **Table lookup**; Telecommunication traffic; Telecommunication **links**; Algorithms; Congestion control (communication); Optimization

Identifiers: Internet protocols (IP); World wide web (WWW); Mutating binary search

Classification Codes:

722.3 (Data Communication, Equipment & Techniques); 723.1 (Computer Programming); 921.5 (Optimization Techniques)
723 (Computer Software); 716 (Radar, Radio & TV Electronic Equipment);
722 (Computer Hardware); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

22/5/13 (Item 4 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

04615046 E.I. No: EIP97023525645

Title: Layout of virtual paths in ATM networks

Author: Gerstel, Ornan; Cidon, Israel; Zaks, Shmuel

Corporate Source: Computer Science Dep, Haifa, Isr

Source: IEEE/ACM Transactions on Networking v 4 n 6 Dec 1996. p 873-884

Publication Year: 1996

CODEN: IEANEP ISSN: 1063-6692

Language: English

Document Type: JA; (Journal Article) Treatment: G; (General Review); T; (Theoretical)

Journal Announcement: 9704W1

Abstract: We study the problem of designing a layout of virtual paths (VP's) on a given ATM network. We first define a mathematical model that captures the characteristics of virtual paths. In this model, we define the general VP layout problem, and a **more** restricted case; while the general case layout should cater connections between any pair of nodes in the network, the restricted case layout should only cater connections between a specific node to the other nodes. For the latter case, we present an algorithm that finds a layout by decomposing the network into subnetworks and operating on each subnetwork, recursively; we prove an upper bound on the optimality of the resulting layout and a **matching** lower bound for the problem, that are tight under certain realistic assumptions. Finally, we show how the solution for the restricted case is used as a building **block** in various solutions to **more** general cases (trees, meshes, K-separable networks, and general topology networks) and prove a lower bound for some of our results. The results exhibit a tradeoff between the efficiency of the call setup and both the utilization of the VP **routing tables** and the overhead during recovery from **link** disconnections. (Author abstract) 27 Refs.

Descriptors: Asynchronous transfer mode; Telecommunication **links** ; Communication channels (information theory); Mathematical models; Algorithms; Boundary value problems; Broadband networks; Problem solving

Identifiers: Virtual paths (VP) layout

Classification Codes:

716.1 (Information & Communication Theory); 921.6 (Numerical Methods)

716 (Radar, Radio & TV Electronic Equipment); 718 (Telephone & Line Communications); 921 (Applied Mathematics)

71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

22/5/14 (Item 5 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

04609920 E.I. No: EIP97013500004

Title: Bi-directional 3-port ATM CAM supporting fast look-up and reduced cycle time

Author: Park, Yeong-Ho

Corporate Source: ETRI, Taejon, S Korea

Conference Title: Proceedings of the 1996 2nd International Conference on ASIC

Conference Location: Shanghai, China Conference Date: 19961021-19961024

Sponsor: IEEE

E.I. Conference No.: 45949

Source: International Conference on ASIC, Proceedings 1996. Shanghai Scientific and Technological Literature Publishing House, Shanghai, China. p 159-162

Publication Year: 1996

CODEN: 002513

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9703W3

Abstract: This paper presents an architecture of a bi-directional 3-port ATM CAM. It satisfies one of the fundamental requirements that ATM cell header translation has to be performed in real time. It also reduces the access cycle time to get a retrieval header and to return the header converted as a result of the **match** processing. The proposed architecture is composed of three access ports. Each port operates independently with

each other. To realize this support function, a bit architecture based on the presented requirements of the functional ATM CAM is proposed. Using such a bit architecture, an architecture of CAM part which includes each module for GFC, VPI, VCI, and PTI field, is also proposed. To provide bi-directional translation of VPI/VCI, two CAM architectures for receiving and transmitting directions are used in each **block** respectively. The two CAMs reciprocates their **matching addresses** and the **data** corresponding to the **addresses**. It provides control cell **extraction** such as OAM, unassigned, and physical layer cells. It optionally provides 3 bytes tagging for cell switching function for both UNI and NNI modes. (Author abstract) 4 Refs.

Descriptors: **Data** storage equipment; Asynchronous transfer mode; Response time (computer systems); **Table lookup**; Real time systems; Switching functions; **Data** communication systems; VLSI circuits

Identifiers: Access cycle time; Access ports; Control cell **extraction**

Classification Codes:

722.1 (Data Storage, Equipment & Techniques); 716.1 (Information & Communication Theory); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 714.2 (Semiconductor Devices & Integrated Circuits)

722 (Computer Hardware); 716 (Radar, Radio & TV Electronic Equipment); 723 (Computer Software); 721 (Computer Circuits & Logic Elements); 714 (Electronic Components)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

22/5/15 (Item 6 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

04592973 E.I. No: EIP97013489663

Title: M68HC12 addressing mode and instruction set improvements

Author: Bannatyne, Ross

Corporate Source: Motorola AMCU, Austin, TX, USA

Source: Electronic Engineering (London) v 68 n 838 Oct 1996. 4p

Publication Year: 1996

CODEN: ELEGAP ISSN: 0013-4902

Language: English

Document Type: JA; (Journal Article) Treatment: G; (General Review); T; (Theoretical)

Journal Announcement: 9703W1

Abstract: The M68HC12 microcontroller has been announced as a migration path for users of the M68HC11. Although the M68HC12 retains many similarities to the M68HC11, made to allow source code reuse, some improvements to the **addressing** modes and instruction set are discussed. These improvements are as follows: enhancing **addressing** capabilities, improving index and pointer calculations, automatic pre/post-increment/decrement indexed **addressing** modes, **new** instructions for efficient bank-switched memory, comprehensive transfer and exchange instructions, addition of move instructions, fast maths/arithmetic operations, fuzzy logic and complex **control** instructions, **table look-up** and interpolation, and background instruction.

Descriptors: Microprocessor chips; Computer control; Mathematical programming; **Data** storage equipment; Switching; Fuzzy sets; Computer programming languages; **Table lookup**

Identifiers: Microcontrollers; Embedded systems

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 731.5 (Robotics); 723.1 (Computer Programming); 921.5 (Optimization Techniques); 722.1 (Data Storage, Equipment & Techniques)

714 (Electronic Components); 723 (Computer Software); 731 (Automatic Control Principles); 921 (Applied Mathematics); 722 (Computer Hardware)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING); 92 (ENGINEERING MATHEMATICS)

22/5/16 (Item 7 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

04364635 E.I. No: EIP96033109562

Title: Routing on longest- matching prefixes

Author: Doeringer, Willibald; Karjoth, Gunter; Nassehi, Mehdi

Corporate Source: FH Worms, Ger

Source: IEEE/ACM Transactions on Networking v 4 n 1 Feb 1996. p 86-96

Publication Year: 1996

CODEN: IEANEP

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications); T;
(Theoretical)

Journal Announcement: 9605W3

Abstract: This article describes the dynamic pre fix tries - a novel **data** structure with algorithms for insertion, deletion, and retrieval to build and maintain a dynamic database of binary keys of arbitrary length. These tries extend the concepts of compact digital (Patricia) tries to support the storage of prefixes and to guarantee retrieval times at most linear in the length of the input key irrespective of the trie size, even when **searching** for longest- **matching** prefixes. The **new** design permits very efficient, simple and nonrecursive implementations of small code size and minimal storage requirements. Insert and delete operations have strictly local effects, and their particular sequence is irrelevant for the structure of the resulting trie, thus maintaining at all times the desired storage and computational efficiency. The algorithms have been successfully employed in experimental communication systems and products for a variety of networking functions such as **address** resolution, maintenance and verification of access control lists, and high-performance **routing tables** in operating system kernels. (Author abstract) 28 Refs.

Descriptors: Computer networks; **Data** structures; Algorithms; Database systems; Computer operating systems; Computational complexity; Binary sequences

Identifiers: Algorithmic complexity; Delete operation; Insert operation

Classification Codes:

723.5 (Computer Applications); 723.2 (Data Processing); 723.3 (Database Systems); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)

723 (Computer Software); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING)

22/5/17 (Item 8 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

04346290 E.I. No: EIP96023023964

Title: New SRAM-based FPGA architectures address new applications

Author: Fawcett, Bradley K.

Corporate Source: Xilinx Inc, San Jose, CA, USA

Conference Title: Proceedings of the 1995 Wescon Conference

Conference Location: San Francisco, CA, USA Conference Date: 19951107-19951109

Sponsor: IEEE; ERA

E.I. Conference No.: 44303

Source: Wescon Conference Record 1995. Wescon, Los Angeles, CA, USA, 95CB35791. p 231-236

Publication Year: 1995

CODEN: WCREDI

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T;
(Theoretical)

Journal Announcement: 9604W1

Abstract: To better meet the varying needs and **further** expand the range of applications that can be **addressed** by FPGA technology, Xilinx has recently introduced several **new** SRAM-based FPGA products. These **new**

product offerings reflect the goal of every electronics design: leverage advancing technology to best **match** users' needs. In some cases, this takes the form of evolutionary improvements to current products, such as performance improvements for the XC3100A FPGA family and enhancements to the XC4000 FPGA architecture to create the XC4000E family. In other cases, it involves **new** product development to take full advantage of **new** technologies and emerging applications, as with the **new** XC5000 and XC6200 FPGA families. 4 Refs.

Descriptors: *Logic design; Random access storage; Application specific integrated circuits; Software engineering; Interfaces (computer); Digital arithmetic; Shift registers; Transistor transistor logic circuits; CMOS integrated circuits; Formal logic

Identifiers: Static random access memory; Field programmable gate array; Video controllers; Image processors; Configurable logic **block** ; Totem pole structure; General **routing matrix** ; Local interconnect matrix

Classification Codes:

721.2 (Logic Elements); 722.1 (Data Storage, Equipment & Techniques); 714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 722.2 (Computer Peripheral Equipment); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)

721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 714 (Electronic Components); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

22/5/20 (Item 11 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

03881250 E.I. No: EIP94061321496

Title: Fast implementation of a perfect hash function for picture objects

Author: Bhatia, Sanjiv K.; Sabharwal, Chaman L.

Corporate Source: Univ of Missouri-St Louis, St Louis, MO, USA

Source: Pattern Recognition v 27 n 3 Mar 1994. p 365-376

Publication Year: 1994

CODEN: PTNRA8 ISSN: 0031-3203

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 9408W1

Abstract: In image database systems, symbolic pictures are represented by two-dimensional (2D) strings that are converted into triples. Each triple is mapped to a unique hash **address** for timely retrieval of pictures, reducing the pattern-**matching** problem **corresponding** to a **query** to that of computation of a hash function. The values associated with the picture **objects** are used to compute hash **addresses** for triples developed from the query. Heuristics are proposed to speed up the computation of the associated values for the picture **objects** . Experimental results show that the **new** algorithm achieves almost a 90% gain, in search space, over existing algorithms to compute the associated values. (Author abstract) 19 Refs.

Descriptors: Database systems; Pattern recognition; Image processing; Information retrieval; Query languages; Computation theory; Algorithms; Heuristic methods; Online searching; **Table lookup**

Identifiers: Image database system; Two dimensional string; Perfect hashing function; Associated value function; Picture **object** ; Triples; Pattern **matching** problem

Classification Codes:

723.3 (Database Systems); 723.2 (Data Processing); 903.3 (Information Retrieval & Use); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 921.6 (Numerical Methods)

723 (Computer Software); 903 (Information Science); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics)

72 (COMPUTERS & DATA PROCESSING); 90 (GENERAL ENGINEERING); 92 (ENGINEERING MATHEMATICS)

22/5/21 (Item 12 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

03810285 E.I. No: EIP94021217671

Title: **FLASH: a fast look-up algorithm for string homology**

Author: Califano, Andrea; Rigoutsos, Isidore

Corporate Source: IBM T.J. Watson Research Cent, Yorktown Heights, NY, USA

Conference Title: Proceedings of the 1993 IEEE Computer Society Conference on Computer Vision and Pattern Recognition

Conference Location: New York, NY, USA Conference Date: 19930615-19930618

Sponsor: IEEE

E.I. Conference No.: 18886

Source: IEEE Computer Vision and Pattern Recognition Proc 1993 IEEE Comput Soc Conf Comput Vision Pattern Recognit 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA, (IEEE cat n 93CH3309-2). p 353-359

Publication Year: 1993

ISBN: 0-8186-3882-6

Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review); T; (Theoretical); A; (Applications)

Journal Announcement: 9404W3

Abstract: We are in the middle of a long-range worldwide race to map and sequence the genome of Homo sapiens and that of many other living creatures. About 10^{*8} nucleotides and aminoacids of mammals, primates, rodents, bacteria, and other life forms have already been classified and stored in publicly available database such as Genbank. By the end of the century we should be close to the estimated mark of 1 billion nucleotides. A key issue in managing such large amounts of **data** is the availability of efficient, accurate, and selective techniques to detect homology (similarity) between newly recovered and previously acquired sequences. Unfortunately, even today's most advanced algorithms such as Smith-Waterman, FASTA and BLAST, are designed to scan the contents of the entire database for one or **more matches**. This results in long search times or in a sharp tradeoff between accuracy and amount of computation. The algorithm we present here is based on a probabilistic indexing framework which requires minimal access to the database for such **match**. A highly redundant number of descriptive tuples from the sequences of interest are generated and used as indices in **table look - up** paradigm. Theoretical and experimental results on the sensitivity and accuracy of the approach are provided. This includes the probability of correct and random **matches** and the storage and computational requirements. An experimental system has been implemented for a database containing the complete genome of the bacteria E.Coli (approximately 2 million nucleotides). The system is being expanded to include the complete Genbank database. Search time is of a few seconds on a workstation class machine. The algorithm is shown to scale well to databases containing billions of nucleotides with performances that are orders of magnitude better even than BLAST, the fastest of the current techniques. The approach is of a very general nature and is being applied to a large number of other **domains** and **data** topologies such as speech recognition, sound and image databases. (Author abstract) 10 Refs.

Descriptors: Pattern recognition; Mathematical models; Algorithms; **Table lookup**; **Data** processing; Database systems; Speech recognition

Identifiers: String homology; Fast lookup algorithm FLASH; Nucleotides; Genome mapping; Probabilistic framework; Genbase

Classification Codes:

723.2 (Data Processing); 723.3 (Database Systems)

723 (Computer Software); 921 (Applied Mathematics)

72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

22/5/22 (Item 13 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)
(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

02244850 E.I. Monthly No: EIM8704-029037

Title: **DIGITAL SCAN CONVERTER FORWARD LOOKING INFRARED (FLIR) CHARACTERIZATION.**

Author: Holst, Gerald C.

Corporate Source: Martin Marietta Aerospace, Orlando, FL, USA

Conference Title: Thermal Imaging.

Conference Location: Orlando, FL, USA Conference Date: 19860403

Sponsor: SPIE, Bellingham, WA, USA; Univ of Alabama, Cent for Applied Optics, Huntsville, AL, USA; Univ of Dayton, Cent for Electro-Optics, Dayton, OH, USA; Georgia Inst of Technology, Atlanta, GA, USA; Univ of Rochester, Inst of Optics, Rochester, NY, USA; Univ of Arizona, Optical Sciences Cent, Tucson, AZ, USA

E.I. Conference No.: 09010

Source: Proceedings of SPIE - The International Society for Optical Engineering v 636. Publ by SPIE, Bellingham, WA, USA p 80-84

Publication Year: 1986

CODEN: PSISDG ISSN: 0277-786X ISBN: 0-89252-671-8

Language: English

Document Type: PA; (Conference Paper)

Journal Announcement: 8704

Abstract: A **parallel** scan forward looking infrared (FLIR) with a digital scan converter (DSC) electronically reformats parallel input analog **data** into serial digital output **data**. This digital **data** can be supplied directly to a subsystem for **further** processing. Prior to returning to the analog **domain** to create the video image, the digital **data** passes through a line-to-line interpolation operator, gamma correction **look up table** and a histogram processor. Because of the video processing, the characteristics of the analog signal is different than the digital signal. Since the characteristics are different, it is essential to measure the system intensity transfer function (SITF), and noise equivalent temperature difference (NEDT) in both the analog and digital **domains**. Appropriate digital **data** display (histogram of values) permits easy assessment of **data** quality. Examples of missing **data** bits (dead lines) are shown. Lower order missing bits can affect a subsystem but the effect is minimized on the display due to the line-to-line interpolation scheme. The NEDT, SITF and noise spectral density in the digital and analog **domains** are compared. The implications of the difference in both **domains** are discussed. (Edited author abstract)

Descriptors: *IMAGE PROCESSING--*Image Analysis; SIGNAL PROCESSING--Digital Techniques; INFRARED IMAGING

Identifiers: THERMAL IMAGING SYSTEMS

Classification Codes:

723 (Computer Software); 741 (Optics & Optical Devices)

72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY)

22/5/23 (Item 1 from file: 2)

DIALOG(R) File 2: INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6512632 INSPEC Abstract Number: B2000-04-6150M-010, C2000-04-5640-010

Title: IP address **lookup made fast and simple**

Author(s): Crescenzi, P.; Dardini, L.; Grossi, R.

Author Affiliation: Dept. of Syst. & Inf., Florence Univ., Italy

Conference Title: Algorithms - ESA'99. 7th Annual European Symposium. Proceedings (Lecture Notes in Computer Science Vol.1643) p.65-76

Editor(s): Nesetril, J.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 1999 Country of Publication: Germany xii+552 pp.

ISBN: 3 540 66251 0 Material Identity Number: XX-1999-02389

Conference Title: Algorithms - ESA'99. 7th Annual European Symposium

Conference Date: 16-18 July 1999 Conference Location: Prague, Czech Republic

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Theoretical (T); Experimental (X)

Abstract: The **IP address** lookup problem is one of the major bottlenecks in high-performance routers. Previous solutions to this problem first describe it in the general terms of longest prefix **matching** and, then, are experimented on real **routing tables** **T**. We follow the opposite direction. We start out from the experimental analysis of real **data** and, based upon our findings, we provide a **new** and simple solution to the **IP address** lookup problem. **More** precisely, our solution for **m-bit IP addresses** is a reasonable trade-off between performing a binary search on **T** with $O(\log T)$ accesses, where **T** is the number of entries in **T**, and executing a single access on a table of $2^{\lceil m/2 \rceil}$ entries obtained by fully expanding **T**. While the previous results start out from space-efficient **data** structures and aim at lowering the $O(\log T)$ access cost, we start out from the expanded table with $2^{\lceil m/2 \rceil}$ entries and aim at compressing it without an excessive increase in the number of accesses. Our algorithm takes exactly three memory accesses and occupies $O(2^{\lceil m/2 \rceil} \cdot T^2)$ space in the worst case. Experiments on real **routing tables** for **m=32** show that the space bound is overly pessimistic. Our solution occupies approximately one megabyte for the MaeEast **routing table** (which has **T** approximately=44000 and requires approximately 250 KB) and, thus, takes three cache accesses on any processor with 1 MB of L2 cache. According to the measurement obtained by the VTune tool on a Pentium II processor, each lookup requires 3 **additional** clock cycles besides the ones needed for the memory accesses. Assuming a clock cycle of 3.33 nanoseconds and an L2 cache latency of 15 nanoseconds, search of MaeEast can be estimated in 55 nanoseconds or, equivalently, our method performs 18 million lookups per second. (17 Refs)

Subfile: B C

Descriptors: cache storage; computational complexity; **data** structures; Internet; protocols; search problems; **table lookup**; telecommunication network routing

Identifiers: **IP address** lookup; high-performance routers; binary search; space-efficient **data** structures; access cost; space bound; cache accesses; L2 cache; VTune tool; Pentium II processor; cache latency; MaeEast search

Class Codes: B6150M (Protocols); B6210L (Computer communications); B6150P (Communication network design, planning and routing); B0250 (Combinatorial mathematics); C5640 (Protocols); C5620W (Other computer networks); C1160 (Combinatorial mathematics); C5670 (Network performance)

Copyright 2000, IEEE

22/5/24 (Item 2 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6497052 INSPEC Abstract Number: B2000-03-1265D-039, C2000-03-5340-006

Title: Pseudo 3-way set-associative cache: a way of reducing miss ratio with fast access time

Author(s): Yongjoon Lee; Byung-Kwon Chung

Author Affiliation: Dept. of Comput. & Inf. Sci. & Eng., Florida Univ., Gainesville, FL, USA

Conference Title: Engineering Solutions for the Next Millennium. 1999 IEEE Canadian Conference on Electrical and Computer Engineering (Cat. No.99TH8411) Part vol.1 p.391-6 vol.1

Editor(s): Meng, M.

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 3 vol. (xxiii+1758) pp.

ISBN: 0 7803 5579 2 Material Identity Number: XX-1999-02278

U.S. Copyright Clearance Center Code: 0 7803 5579 2/99/\$10.00

Conference Title: Engineering Solutions for the Next Millennium. 1999 IEEE Canadian Conference on Electrical and Computer Engineering

Conference Date: 9-12 May 1999 Conference Location: Edmonton, Alta., Canada

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: The multiple-access cache is a direct-mapped cache that may be accessed **more** than once, each time with a different hash function, to satisfy a memory request. A fast access time can be achieved when the requested **data** is found at the direct-mapped location, while a high overall hit ratio can be accomplished with the **additional** cache access. To prevent long delays in accessing the alternative location, the multiple-access cache generally accesses the cache at most twice. Thus, the hit ratio of the multiple-access cache has a limitation of that of 2-way set-associative cache. In this paper, a pseudo 3-way set-associative cache is proposed. The pseudo 3-way set-associative cache searches the direct-mapped location and one alternative location, if necessary, to **find** a **match**. The pseudo 3-way set-associative cache can overcome the limitation of the hit ratio of 2-way set-associative cache with at most two searches from a fast direct-mapped cache. To achieve this goal, the pseudo 3-way set-associative cache uses small **tables** indicating different **hash** functions to search the alternative location. With **additional** 1.5 bits per cache line, we can achieve a hit ratio approaching that of a 4-way set-associative cache. (14 Refs)

Subfile: B C

Descriptors: cache storage; content- **addressable** storage; delays

Identifiers: pseudo 3-way set-associative cache; cache miss ratio; cache access time; multiple-access cache; direct-mapped cache; hash functions; memory request; hit ratio; tables; hash-rehash cache; column-associative cache; cache performance

Class Codes: B1265D (Memory circuits); C5340 (Associative storage); C5320G (Semiconductor storage); C6120 (File organisation)

Copyright 2000, IEE

22/5/25 (Item 3 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6393143 INSPEC Abstract Number: B1999-12-6210L-057, C1999-12-5620W-034

Title: At the core of IP networks: link -state routing protocols

Author(s): Metz, C.

Journal: IEEE Internet Computing vol.3, no.5 p.72-7

Publisher: IEEE,

Publication Date: Sept.-Oct. 1999 Country of Publication: USA

CODEN: IICOFX ISSN: 1089-7801

SICI: 1089-7801(199909/10)3:5L:72:CNLS;1-F

Material Identity Number: F277-1999-005

U.S. Copyright Clearance Center Code: 1089-7801/99/\$10.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: As end users and managers of both corporate and Internet service provider (ISP) IP networks, we ask a lot of those devices called routers. They must be reliable and easy to manage, while supporting a variety of LAN and WAN interfaces at a reasonable price. They must forward hundreds of thousands or even millions of **packets** per second. For each **packet**, this means the router receives it, **extracts** the destination **address** contained in the header, performs a lookup in a local **routing table**, **finds** the best **match**, and then transmits the **packet** to the next-hop router. The router may even be configured to examine **additional** fields in the **packet** and, based on this analysis, decide whether to place the **packet** in a high-priority transmission queue for expedited service. The author discusses **link -state routing protocols**. (10 Refs)

Subfile: B C

Descriptors: Internet; telecommunication network routing; transport protocols

Identifiers: IP networks; **link -state routing protocols**; Internet service provider; LAN; WAN; price; destination **address**; **table lookup**

Class Codes: B6210L (Computer communications); B6150M (Protocols); B6150P (Communication network design, planning and routing); C5620W (Other computer networks); C5640 (Protocols)

Copyright 1999, IEE

22/5/26 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6385576 INSPEC Abstract Number: B1999-12-6210L-007, C1999-12-5620W-005

Title: Fast IP routing lookups for high performance routers

Author(s): Kijkanjanarat, T.; Chao, H.J.

Author Affiliation: Dept. of Electr. Eng., Polytech. Univ., Brooklyn, NY, USA

Journal: Computer Communications vol.22, no.15-16 p.1415-22

Publisher: Elsevier,

Publication Date: 25 Sept. 1999 Country of Publication: Netherlands

CODEN: COCOD7 ISSN: 0140-3664

SICI: 0140-3664(19990925)22:15/16L.1415:FRLH;1-X

Material Identity Number: H089-1999-017

U.S. Copyright Clearance Center Code: 0140-3664/99/\$20.00

Document Number: S0140-3664(99)00099-7

Language: English Document Type: Journal Paper (JP)

Treatment: Theoretical (T)

Abstract: The key to the success of the next generation IP networks to provide good services relies on the deployment of high performance routers to do fast IP routing lookups. In this paper, we propose a **new** algorithm for fast IP lookups using a so-called two-trie structure. The two-trie structure provides the advantages in that less memory space is required for representing a **routing table** than the standard trie while it still provides fast LP lookups. Based on the simulation result, the memory space can be saved around 27% over the standard trie while a lookup operation takes 1.6 memory accesses in the average case and 8 memory accesses in the worst case. Also, the structure is not based on any assumptions about the distribution of the prefix lengths in **routing tables**. Thus, increasing the lengths from 32 to 128 bit (from IPv4 to IPv6) does not affect the main structure. (12 Refs)

Subfile: B C

Descriptors: Internet; transport protocols; tree **data** structures

Identifiers: IP routing lookups; high performance routers; next generation IP networks; two-trie structure; **IP address** lookup; longest **matching** prefix; trie

Class Codes: B6210L (Computer communications); B6150M (Protocols); C5620W (Other computer networks); C5640 (Protocols)

Copyright 1999, IEE

22/5/27 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6346028 INSPEC Abstract Number: B1999-10-6150P-039, C1999-10-6130-007

Title: A fast IP routing lookup scheme for gigabit switching routers

Author(s): Nen-Fu Huang; Shi-Ming Zhao; Jen-Yi Pan; Chi-An Su

Author Affiliation: Dept. of Comput. Sci., Nat. Tsing Hua Univ., Hsinchu, Taiwan

Conference Title: IEEE INFOCOM '99. Conference on Computer Communications. Proceedings. Eighteenth Annual Joint Conference of the IEEE Computer and Communications Societies. The Future is Now (Cat. No.99CH36320) Part vol.3 p.1429-36 vol.3

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 3 vol. xxv+1583 pp.

ISBN: 0 7803 5417 6 Material Identity Number: XX-1999-00751

U.S. Copyright Clearance Center Code: 0 7803 5417 6/99/\$10.00

Conference Title: Proceedings of INFOCOM'99: Conference on Computer Communications

Conference Sponsor: IEEE Comput. Soc.; IEEE Commun. Soc

Conference Date: 21-25 March 1999 Conference Location: New York, NY, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); New Developments (N); Practical (P)

Abstract: One of the key design issues for the new generation IP routers is the route lookup mechanism. For each incoming IP packet, the IP routing requires to perform a longest prefix matching on the address lookup in order to determine the packet's next hop. This paper presents a fast route lookup mechanism that only needs tiny SRAM and can be implemented in a pipelined skill in hardware. Based on the proposed scheme, the forwarding table is tiny enough to fit in SRAM with very low cost. For example, a large routing table with 40,000 routing entries can be compacted to a forwarding table of 450-470 Kbytes. In the worst case, the number of memory accesses for a lookup is three. When implemented in a pipeline skill in hardware, the proposed mechanism can achieve one routing lookup every memory access. With current 10 ns SRAM, this mechanism furnishes approximately 100 million routing lookups per second. This is much faster than any current commercially available routing lookup schemes. (13 Refs)

Subfile: B C

Descriptors: electronic switching systems; pipeline processing; SRAM chips; table lookup; telecommunication network routing; transport protocols

Identifiers: fast IP routing lookup; gigabit switching routers; IP packet; longest prefix matching; address lookup; SRAM; pipelined hardware; forwarding table; memory accesses; 450 to 470 kbyte; 10 ns

Class Codes: B6150P (Communication network design, planning and routing); B6150M (Protocols); B1265D (Memory circuits); B6230B (Electronic switching systems and exchanges); C6130 (Data handling techniques); C5640 (Protocols); C5320G (Semiconductor storage); C5220P (Parallel architecture)

Numerical Indexing: memory size 4.6E+05 to 4.8E+05 Byte; time 1.0E-08 s

Copyright 1999, IEE

22/5/28 (Item 6 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6129962 INSPEC Abstract Number: B1999-02-6150P-018, C1999-02-5620W-020

Title: Fast IP routing with LC-tries

Author(s): Nilsson, S.; Karlsson, G.

Author Affiliation: Helsinki Univ., Finland

Journal: Dr. Dobbs's Journal vol.23, no.8 p.70, 72-5

Publisher: Miller Freeman,

Publication Date: Aug. 1998 Country of Publication: USA

CODEN: DDJSDM ISSN: 1044-789X

SICI: 1044-789X(199808)23:8L:70:FRWT;1-P

Material Identity Number: B719-1998-012

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: One of the bottlenecks of the Internet is the address lookup operations performed by the routers. Expensive tailor-made hardware solutions have typically been used to achieve the necessary speed. In this article, we show that it is possible to perform the lookups efficiently with a simple data structure-a level-compressed (LC) trie. A software implementation can sustain several million lookups per second, enough to match a Gbit/s link. The data structure is simple and it scales well. No modifications are needed when switching from the 32-bit addresses of IP version 4 (IPv4) to the 128-bit addresses of IP version 6 (IPv6), and we expect the lookup operation to be almost as fast for the longer addresses. Address lookup in IPv4 is easy. Since only the first 24 bits are used by the core routers, a simple bucketing scheme solves the problem. In IPv6, the addresses are longer and one needs more sophisticated methods. We believe that the LC-trie is a suitable data structure. It's simple and compact and an address lookup requires only a few memory accesses. The depth of the structure does not depend on the length of the strings and grows slowly as a function of the number of entries in the table. (0 Refs)

Subfile: B C

Descriptors: data compression; data structures; Internet; table

lookup ; telecommunication network routing; transport protocols
Identifiers: fast IP routing; LC-tries; Internet; **address** lookup
operations; **data** structure; level-compressed trie; software
implementation; Gbit/s **link** ; 32-bit **addresses** ; IP version 4; 128-bit
addresses ; IP version 6; core routers; bucketing scheme; memory accesses;
string length

Class Codes: B6150P (Communication network design, planning and routing);
B6150M (Protocols); B6210L (Computer communications); C5620W (Other
computer networks); C5640 (Protocols); C7210N (Information networks);
C6120 (File organisation)
Copyright 1999, IEE

22/5/29 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6112349 INSPEC Abstract Number: C9901-5630-006

Title: FPGA-based Internet Protocol Version 6 router

Author(s): Mansour, M.; Kayssi, A.

Author Affiliation: Dept. of Electr. & Comput. Eng., American Univ. of
Beirut, Lebanon

Conference Title: Proceedings International Conference on Computer
Design. VLSI in Computers and Processors (Cat. No.98CB36273) p.334-9

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1998 Country of Publication: USA xix+644 pp.

ISBN: 0 8186 9099 2 Material Identity Number: XX98-02930

U.S. Copyright Clearance Center Code: 0 8186 9099 2/98/\$10.00

Conference Title: Proceedings International Conference on Computer
Design. VLSI in Computers and Processors

Conference Sponsor: IEEE Comput. Soc.; IEEE Circuits & Syst. Soc.; IEEE
Electron Devices Soc

Conference Date: 5-7 Oct. 1998 Conference Location: Austin, TX, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: In this paper, a novel hardware design for an Internet Protocol
Version 6 router using field programmable gate arrays is proposed. A
dataflow, parallel, pipelined and scalable architecture is presented that
has the potential of **matching** the enormous communication bandwidths of
transmission **links** . A ternary content **addressable** memory (CAM) in the
form of cache is adopted as a **routing** **table** search engine. It can offer
O(1) search time with just O(N) memory words. Adding a sorting (priority)
mechanism by caching the **routing** **table** in CAM and using a modified form
of sector mapping technique eliminates the slow insertion and deletion
times without adding significant **additional** hardware costs. (8 Refs)

Subfile: C

Descriptors: **data** flow computing; field programmable gate arrays;
Internet; parallel architectures; transport protocols

Identifiers: hardware design; Internet Protocol; field programmable gate
arrays; scalable architecture; pipelined; parallel; dataflow

Class Codes: C5630 (Networking equipment); C5220P (Parallel architecture
); C5640 (Protocols); C5120 (Logic and switching circuits)

Copyright 1998, IEE

22/5/30 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6105104 INSPEC Abstract Number: B9901-6210L-078, C9901-5620W-025

**Title: High-speed policy-based packet forwarding using efficient
multi-dimensional range matching**

Author(s): Lakshman, T.V.; Stiliadis, D.

Author Affiliation: AT&T Bell Labs., Holmdel, NJ, USA

Journal: Computer Communication Review Conference Title: Comput. Commun.
Rev. (USA) vol.28, no.4 p.203-14

Publisher: ACM,

Publication Date: Oct. 1998 Country of Publication: USA
CODEN: CCRED2 ISSN: 0146-4833
SICI: 0146-4833(199810)28:4L:203:HSPB;1-5
Material Identity Number: B579-98004
Conference Title: ACM SIGCOMM'98 Conference. Applications, Technologies,
Architectures, and Protocols for Computer Communication
Conference Sponsor: ACM
Conference Date: 2-4 Sept. 1998 Conference Location: Vancouver, BC,
Canada
Language: English Document Type: Conference Paper (PA); Journal Paper
(JP)

Treatment: Applications (A); Practical (P); Theoretical (T)

Abstract: The key mechanism that enables service differentiation in a connectionless network is the **packet** classification function that parses the headers of the **packets**, and after determining their context, classifies them based on administrative policies or real-time reservation decisions. **Packet** classification, however, is a complex operation that can become the bottleneck in routers that try to support gigabit link capacities. Hence, many proposals for differentiated services only require classification at lower speed edge routers and also avoid classification based on multiple fields in the **packet** header even if it might be advantageous to service providers. This paper presents a new **packet** classification scheme that, with a worst-case and traffic independent performance metric, can classify **packets**, by checking amongst a few thousand filtering rules, at rates of a million **packets** per second using range **matches** on more than four **packet** header fields. For a special case of classification in two dimensions, an algorithm is presented that can handle more than 128k rules at these speeds in a traffic independent manner. Worst-case performance over average case performance is emphasized because providing differentiated services requires intelligent queueing and scheduling of **packets** that precludes any significant queueing before the differentiating step. The presented filtering or classification schemes can be used to classify **packets** for security policy enforcement, applying resource management decisions, for identification for RSVP reservations, multicast look-ups, and for source-destination and policy based routing. The scalability and performance of the algorithms have been demonstrated by implementation and testing in a prototype system. (28 Refs)

Subfile: B C

Descriptors: Internet; **packet** switching; security of data ; **table** **lookup** ; telecommunication computing; telecommunication network routing

Identifiers: policy-based **packet** forwarding; multi-dimensional range **matching** ; differentiated service provision; Internet service providers; shared network infrastructure; connectionless network; **packet** classification function; **packet** headers; real-time reservation decision; router bottleneck; worst-case performance metric; traffic independent performance metric; filtering rules; **packet** header fields; two dimensional classification; intelligent **packet** queueing; intelligent **packet** scheduling; security policy enforcement; resource management decisions; RSVP reservation; multicast look-up; policy based routing; forwarding engines

Class Codes: B6210L (Computer communications); B6150P (Communication network design, planning and routing); B6150C (Communication switching); C5620W (Other computer networks); C6130S (Data security); C7410F (Communications computing)

Copyright 1998, IEE

22/5/31 (Item 9 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6105103 INSPEC Abstract Number: B9901-6210L-077, C9901-5620W-024

Title: **Fast and scalable layer four switching**

Author(s): Srinivasan, V.; Varghese, G.; Suri, S.; Waldvogel, M.

Author Affiliation: Dept. of Comput. Sci., Washington Univ., St. Louis, MO, USA

Journal: Computer Communication Review Conference Title: Comput. Commun.

Publisher: ACM,

Publication Date: Oct. 1998 Country of Publication: USA

CODEN: CCRED2 ISSN: 0146-4833

SICI: 0146-4833(199810)28:4L:191:FSLF;1-J

Material Identity Number: B579-98004

Conference Title: ACM SIGCOMM'98 Conference. Applications, Technologies, Architectures, and Protocols for Computer Communication

Conference Sponsor: ACM

Conference Date: 2-4 Sept. 1998 Conference Location: Vancouver, BC, Canada

Language: English Document Type: Conference Paper (PA); Journal Paper (JP)

Treatment: Applications (A); Theoretical (T)

Abstract: In layer four switching, the route and resources allocated to a **packet** are determined by the destination **address** as well as other header fields of the **packet** such as source **address**, TCP and UDP port numbers. Layer four switching unifies firewall processing, RSVP style resource reservation filters, QoS routing, and normal unicast and multicast forwarding into a single framework. In this framework, the forwarding database of a router consists of a potentially large number of filters on key header fields. A given **packet** header can **match** multiple filters, so each filter is given a cost, and the **packet** is forwarded using the least cost **matching** filter. In this paper, two **new** algorithms are described for solving the least cost **matching** filter problem at high speeds. Our first algorithm is based on a grid-of-tries construction and works optimally for processing filters consisting of two prefix fields (such as destination-source filters) using linear space. Our second algorithm, cross-producting, provides fast lookup times for arbitrary filters but potentially requires large storage. A combination scheme is described that combines the advantages of both schemes. The combination scheme can be optimized to handle pure destination prefix filters in four memory accesses, destination-source filters in eight memory accesses worst case, and all other filters in eleven memory accesses in the typical case. (32 Refs)

Subfile: B C

Descriptors: database management systems; Internet; **packet** switching; **table lookup**; telecommunication computing; telecommunication network routing; telecommunication traffic

Identifiers: scalable layer four switching; **packet** route allocation; **packet** resources allocation; destination **address**; header fields; source **address**; TCP port numbers; UDP port numbers; firewall processing; RSVP resource reservation filters; QoS routing; unicast forwarding; multicast forwarding; forwarding database; forwarding router database; key header field filter; **packet** header; multiple filter **match**; least cost **matching** filter; grid-of-tries construction; processing filters; prefix fields; destination-source filters; linear space; combination scheme; destination prefix filters; memory access optimisation; Internet; telecommunication traffic

Class Codes: B6210L (Computer communications); B6150C (Communication switching); B6150P (Communication network design, planning and routing); C5620W (Other computer networks); C7410F (Communications computing); C6160 (Database management systems (DBMS))

Copyright 1998, IEE

22/5/32 (Item 10 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6006119 INSPEC Abstract Number: B9810-6150C-028

Title: Adaptive resource management for IP/ATM hybrid switching systems

Author(s): Hao Che; San-qi Li; Lin, A.

Author Affiliation: Dept. of Electr. & Comput. Eng., Texas Univ., Austin, TX, USA

Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA)

Publisher: SPIE-Int. Soc. Opt. Eng;

Publication Date: 1997 Country of Publication: USA

CODEN: PSISDG ISSN: 0277-786X

SICI: 0277-786X(1997)3233L:328:ARMH;1-N

Material Identity Number: C574-98019

U.S. Copyright Clearance Center Code: 0277-786X/97/\$10.00

Conference Title: Broadband Networking Technologies

Conference Sponsor: SPIE

Conference Date: 2-3 Nov. 1997 Conference Location: Dallas, TX, USA

Language: English Document Type: Conference Paper (PA); Journal Paper (JP)

Treatment: Theoretical (T)

Abstract: This paper **addresses** a fundamental problem in resource management for flow-based hybrid switching systems. Such systems aim at efficiently transporting layer 3 connectionless IP traffic over layer 2 connection-oriented ATM switching fabrics. One idea behind flow-based hybrid switching is first to decompose individual IP **packet** streams into flows and then to classify them into short-lived flows and long-lived flows. While the short-lived flows are best forwarded by the embedded software through permanent virtual connections (PVC), the long-lived flows are **more** effectively transmitted by hardware through to-be-established switched virtual connections (SVC). Clearly the flow classification mechanism will have a great impact on the utilization of the system's resources. Unlike the traditional emphasis on resources such as **link** bandwidth and cell buffer size, our paper focuses on the resources which are directly associated with **packet** processing power, signaling capacity and **routing table** size. Our study indicates that the presently available static flow classification methods have a vital shortcoming in balancing the utilization of the system's resources. We propose a novel approach for adaptive flow classification which can balance the utilization of system resources to **match** the time varying traffic characteristics. After formulating the proposed flow adaptation as a stochastic control problem, a heuristic algorithm is developed. The simulation study based on real traces shows the viability of the proposed flow adaptation for dynamic resource management in flow-based hybrid switching system design. (11 Refs)

Subfile: B

Descriptors: adaptive systems; asynchronous transfer mode; buffer storage ; **packet** switching; stochastic processes; telecommunication congestion control; telecommunication network management; telecommunication network routing; telecommunication signalling; telecommunication traffic; transport protocols

Identifiers: IP/ATM hybrid switching systems; adaptive resource management; flow-based hybrid switching; layer 3 connectionless IP traffic; layer 2 connection-oriented switching fabrics; IP **packet** streams; short-lived flows; long-lived flows; embedded software; permanent virtual connections; switched virtual connections; flow classification mechanism; system resources utilization; **link** bandwidth; cell buffer size; **packet** processing; signaling capacity; **routing table** size; static flow classification methods; adaptive flow classification; time varying traffic characteristics; stochastic control problem; heuristic algorithm; simulation study; real traces; dynamic resource management

Class Codes: B6150C (Communication switching); B6150M (Protocols); B6150P (Communication network design and planning); B6210C (Network management); B0240Z (Other topics in statistics)

Copyright 1998, IEE

22/5/37 (Item 15 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

5429503 INSPEC Abstract Number: C9701-6160B-008

Title: Load control in scalable distributed file structures

Author(s): Breitbart, Y.; Vingralek, R.; Weikum, G.

Author Affiliation: Dept. of Comput. Sci., Kentucky Univ., Lexington, KY,

USA

Journal: Distributed and Parallel Databases vol.4, no.4 p.319-54
Publisher: Kluwer Academic Publishers,
Publication Date: Oct. 1996 Country of Publication: Netherlands
CODEN: DPADEH ISSN: 0926-8782
SICI: 0926-8782(199610)4:4L:319:LCSD;1-W
Material Identity Number: P900-96004
U.S. Copyright Clearance Center Code: 0926-8782/96/\$8.50
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)

Abstract: Presents DiFS (Distributed File Structures), a family of file structures for record-structured, disk-resident files with key-based exact- or interval-match access. The file is organized into buckets that are spread among multiple servers, where a server may hold several buckets. Client requests are serviced by mapping keys on to buckets and looking up the corresponding server in an address table. Dynamic growth, in terms of file size and access load, is supported by bucket splits and bucket migrations on to the existing or newly-created servers. The major problem that we are addressing is achieving scalability, in the sense that both the file size and the client throughput can be scaled up by linearly increasing the number of servers and dynamically redistributing the data. Unlike previous work with similar objectives, our data redistribution explicitly considers the cost/performance ratio of the system by aiming to minimize the number of servers that are used to provide the required performance. A new server is added only if the overall server load in the system does not drop below a pre-specified threshold. Simulation results demonstrate the scalability with controlled cost/performance ratio and the importance of global load control. The impact of various tuning parameters on the effectiveness of the load control is studied in detail. Finally, we compare our approach with other approaches known to date and demonstrate that each of the previous approaches can be recast as a special case of our model. (18 Refs)

Subfile: C

Descriptors: client-server systems; data structures; distributed databases; resource allocation; software performance evaluation; table lookup

Identifiers: global load control; scalable distributed file structures; DiFS; record-structured disk-resident files; key-based exact-match access; key-based interval-match access; client-server system; key mapping; address table; dynamic growth; file size; access load; bucket splits; bucket migrations; scalability; client throughput; dynamic data redistribution; controlled cost/performance ratio; server load threshold; tuning parameters; hashing

Class Codes: C6160B (Distributed databases); C6120 (File organisation); C6150N (Distributed systems software)

Copyright 1996, IEE

22/5/39 (Item 17 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

4536001 INSPEC Abstract Number: C9401-5260B-070

Title: Real-time model based vision for industrial domains

Author(s): Seida, S.; Magee, M.

Author Affiliation: Autom. & Data Syst. Div., Southwest Res. Inst., San Antonio, TX, USA

Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.2055 p.17-31

Publication Date: 1993 Country of Publication: USA

CODEN: PSISDG ISSN: 0277-786X

U.S. Copyright Clearance Center Code: 0 8194 1320 8/93/\$6.00

Conference Title: Intelligent Robots and Computer Vision XII: Algorithms and Techniques

Conference Sponsor: SPIE

Conference Date: 7-9 Sept. 1993 Conference Location: Boston, MA, USA

Language: English Document Type: Conference Paper (PA); Journal Paper

(JP)

Treatment: Practical (P)

Abstract: Describes a model based vision system that has been developed which is able to perform model based reasoning at real-time (or near real-time) rates and for which both the hardware and prototyping costs are low. The basic approach taken is to **extract** a set of useful features from observed models using a library of feature primitive operators. Scale and orientation invariant combinations of these features are used as indices into a hardware **lookup table** to establish initial correspondence between similar combinations that will be encountered when examining unknown **objects**. When performing initial recognition of an unknown **object**, evidence for an **object** in a particular spatial pose is accumulated, giving rise to an initial set of hypotheses. The strongest hypotheses are then refined by iteratively hypothesizing **new** (previously uninstantiated) model/**object** feature **matches** and computing a confidence measure associated with the current instantiation set. If confidence increases the newly hypothesized instantiation is retained, otherwise it is discarded. (14 Refs)

Subfile: C

Descriptors: computer vision; feature **extraction**; model-based reasoning; spatial reasoning

Identifiers: computer vision; spatial reasoning; feature **extraction**; model based vision system; model based reasoning; feature primitive operators; hardware **lookup table**; confidence measure; instantiation set

Class Codes: C5260B (Computer vision and picture processing); C6170 (Expert systems)

22/5/42 (Item 2 from file: 202)

DIALOG(R) File 202:Info. Sci. & Tech. Abs.

(c) 2003 EBSCO Publishing. All rts. reserv.

2502150

Adaptive communication, January 1970-December 1989.

Book Title: Report No: PB90-855792/HCW

Corporate Source: National Technical Information Service, Springfield, VA (156 pages)

Publication Date: Jan 1990

Language: English

Document Type: Book Chapter

Record Type: Abstract

Journal Announcement: 2500

This bibliography contains citations concerning techniques to maintain electronic communication when noise, jamming, interference, or atmospheric variables tend to degrade the signal. Electronic communications include radar operation, satellite **data links**, tactical communications, and network communications. Solutions include adaptive **routing**, adaptive antenna **arrays**, and adaptive telecommunication equipment using **matched** filters, coding, phase modulation, delta modulation, spread spectrum, and digital techniques. (This updated bibliography contains 286 citations, 19 of which are **new** entries to the previous edition.)

Descriptors: Bibliographies; Communications; Electronic communication; Noise (information retrieval)

Classification Codes and Description: 3.11 (Communications and

Telecommunications Systems); 1.01 (Primary and **Secondary** Sources)

Main Heading: Information Generation and Promulgation; Information Science and **Documentation**

22/5/43 (Item 3 from file: 202)

DIALOG(R) File 202:Info. Sci. & Tech. Abs.

(c) 2003 EBSCO Publishing. All rts. reserv.

2401437

Adaptive communication, January 1970-December 1988.

Book Title: Report No: PB89-853212/HCW

that switched networks can provide dedicated bandwidth to users, resulting in desktop computing being used in new ways. Indicates that ATM standards are still evolving, and that ATM's main competitors, switched Ethernet and Fast Ethernet, rely on higher-level standards to provide traffic control. Advises looking into such issues as: how upgradable is the vendor's product and can it support evolving standards; how many virtual circuits can the device support; for switches, how much time is required to build and tear down virtual circuits; and for modular switches, if there is support for various speeds and wiring support. Attention is given to Available Bit Rate and other congestion-control mechanisms for use on wide-area links; and Multiprotocol Over ATM, which uses a route server that builds routing tables and pushes them down to switches. Includes two photos. (jo)

Descriptors: Asynchronous Transfer Mode; Networks; Switches; Standards; Vendor Guide; Ethernet; Data Transmission

22/5/48 (Item 1 from file: 239)

DIALOG(R) File 239:Mathsci

(c) 2003 American Mathematical Society. All rts. reserv.

02583565 MR 96g#68008

Parallel routing algorithms for incomplete hypercube interconnection networks.

Hornig, M. S. (Institute of Computer Science and Information Engineering, National Chiao Tung University, Hsinchu, 300, Taiwan (R.O.C.))

Chen, D. J. (Institute of Computer Science and Information Engineering, National Chiao Tung University, Hsinchu, 300, Taiwan (R.O.C.))

Ku, Kuo Lung

(Chen, Deng Jyi)

Corporate Source Codes: RC-NCT-C; RC-NCT-C

Parallel Comput.

Parallel Computing, 1994, 20, no. 12, 1739--1761. ISSN: 0167-8191

CODEN: PACOEJ

Language: English Summary Language: English

Document Type: Journal

Journal Announcement: 9506

Subfile: MR (Mathematical Reviews) AMS

Abstract Length: LONG (40 lines)

The interested reader is also referred to a closely related paper appearing immediately preceding this one in the journal in question [S. H. Hu and H. L. Chen, Parallel Comput. 20 (1994), no. 12, 1721--1738; see the preceding review], and its review, the first paragraph of which applies equally to this review.

The algorithms in this paper, by contrast, tackle a more complex problem: that of finding the maximum number of parallel paths in incomplete hypercubes. In consequence, the descriptions are significantly longer (1 page vs. 10 lines), although this is partly due to the more space-hungry representation of addresses as n -tuples rather than bit strings.

Three cases of incomplete hypercubes are considered: (i) $I \setminus \text{sp } r \setminus \text{sb } m$, their notation for two complete hypercubes of size r and m , (ii) $I \setminus \text{sp } r \setminus \text{sb } M$, their notation for a complete hypercube of size r and a number of complete hypercubes drawn from the set of complete hypercubes of size 0 through $r-1$, again drawing on work of H. P. Katseff [IEEE Trans. Comput. 37 (1988), no. 5, 604--608; CCA 1988:39776], and (iii) $I \setminus \text{sp } r \setminus \text{sb } A$, their notation for a complete hypercube of size r in which there are arbitrarily distributed faulty nodes. J. R. Armstrong and F. G. Gray [IEEE Trans. Comput. 30 (1981), no. 8, 587--589] have shown that the faulty nodes can be identified if they are less than r in number, thus the third routing algorithm assumes that fewer than r nodes are unreliable. Because of the lack of regular structure in $I \setminus \text{sp } r \setminus \text{sb } A$, the authors propose a trial and error approach to finding parallel paths, beginning with a proof of existence of the paths and moving on to the construction of routing matrices. Two methods are proposed: the first finds i parallel paths of length i ; while the second finds $r-i$ paths of length $i+2$, where i is the cardinality of the set of different dimensions (SDD) between the source and destination nodes in each case (note: for the

constraint on $\$i\$$ in the former, the authors write SSD, rather than SDD, as well as in two other places in the paper, but this term does not appear to be defined, although from context it might denote the same as SDD).

The paper concludes by stating that parallel paths are very useful when there are large amounts of **data** to transfer and also because they increase system fault-tolerance.

Reviewer: Padget, Julian (4-BATH-SM)

Review Type: Signed review

Descriptors: *68M10 -Computer science (For papers involving machine computations and programs in a specific mathematical area, see Section --04 in that area)-Computer system organization-Computer networks (See also 90B12) ; 65Y10 -Numerical analysis-Computer aspects of numerical algorithms -Algorithms for specific classes of architectures

22/5/49 (Item 2 from file: 239)

DIALOG(R) File 239:Mathsci

(c) 2003 American Mathematical Society. All rts. reserv.

02525073 MR 95j#68021

Proceedings of the Sixth Annual ACM-SIAM Symposium on Discrete Algorithms.

Held in San Francisco, California, January 22--24, 1995.

Publ: Association for Computing Machinery (ACM), New York; Society for Industrial and Applied Mathematics (SIAM), Philadelphia, PA,

1995, x+654 pp. ISBN: 0-89871-349-8

Language: English

Document Type: Book; Proceedings

Journal Announcement: 9509

Proceedings: Symposium on Discrete Algorithms,; Symposium: Discrete Algorithms,; San Francisco, CA, 6th Annual ACM-SIAM 6th Annual ACM-SIAM 1995

Subfile: MR (Mathematical Reviews) AMS

Abstract Length: LONG (106 lines)

The Fifth Symposium has been reviewed [MR 95b:68018].\)

The seventy papers in this collection include the following: William Aiello, Sivaramakrishnan Rajagopalan and Ramarathnam Venkatesan, Design of practical and provably good random number generators (1--9); Gene Myers and Webb Miller, Chaining multiple-alignment fragments in sub-quadratic time (38--47); Sampath Kannan, Tandy Warnow and Shibu Yooseph, Computing the local consensus of trees (68--77); Alexander V. Karzanov [A. V. Karzanov] and S. Thomas McCormick, Polynomial methods for separable convex optimization in unimodular spaces (78--87); Harold N. Gabow, Algorithms for graphic polymatroids and parametric s-sets (88--97); Maurice Queyranne, A combinatorial algorithm for minimizing symmetric submodular functions (98--101); Dimitris Bertsimas and Chung-Piaw Teo, From valid inequalities to heuristics: a unified view of primal-dual approximation algorithms in covering problems (102--111); Xiao Zhou and Takao Nishizeki, Finding optimal edge-rankings of trees (122--131); Wayne Eberly, Efficient parallel computations for singular band matrices (132--138); Yi-Jen Chiang, Michael T. Goodrich, Edward F. Grove, Roberto Tamassia, Darren Erik Vengroff and Jeffrey Scott Vitter, External-memory graph algorithms (139--149); Magnus M. Halldorsson, Kazuo Iwano, Naoki Katoh and Takeshi Tokuyama, Finding subsets maximizing minimum structures (150--159).

Magnus M. Halldorsson, Approximating discrete collections via local improvements (160--169); Neal E. Young, Randomized rounding without solving the linear program (170--178); George S. Lueker, Average-case analysis of off-line and on-line knapsack problems (179--188); Marshall Bern, Paul Chew [L. Paul Chew], David Eppstein and Jim Ruppert, Dihedral bounds for mesh generation in high dimensions (189--196); L. Paul Chew, Klara Kedem, Micha Sharir, Boaz Tagansky and Emo Welzl, Voronoi diagrams of lines in $\$3\$$ -space under polyhedral convex distance functions (197--204); Karen Daniels and Victor J. Milenkovic, Multiple translational containment: approximate and exact algorithms (205--214); Gautam Das, Giri Narasimhan and Jeffrey Salowe, A new way to weigh malnourished Euclidean graphs (215--222); Stephen Guattery and Gary L. Miller, On the performance of spectral graph partitioning methods (233--242); David K. Maslen and Daniel N. Rockmore,

Adapted diameters and the efficient computation of Fourier transforms on finite groups (253--262); Paul B. Callahan and S. Rao Kosaraju, Algorithms for dynamic closest pair and n -body potential fields (263--272).

Jean-Daniel Boissonnat, Jurek Czyzowicz [Jerzy Czyzowicz], Olivier Devillers and Mariette Yvinec, Circular separability of polygon (273--281); Timothy M. Y. Chan, Jack Snoeyink and Chee-Keng Yap, Output-sensitive construction of polytopes in four dimensions and clipped Voronoi diagrams in three (282--291); Danny Z. Chen, On the all-pairs Euclidean short path problem (292--301); Ye. Dinitz [E. A. Dinitz] and A. Vainshtein, Locally orientable graphs, cell structures, and a new algorithm for the incremental maintenance of connectivity carcasses (302--311); David Alberts and Monika Rauch Henzinger, Average case analysis of dynamic graph algorithms (312--321); Robert Cimikowski, An analysis of some heuristics for the maximum planar subgraph problem (322--331); R. Ravi and David P. Williamson, An approximation algorithm for minimum-cost vertex-connectivity problems (332--341); E. Knill, Lower bounds for identifying subset members with subset queries (369--377); Sairam Subramanian and Sridhar Ramaswamy, The P -range tree: a new data structure for range searching in secondary memory (378--387); Jeff Erickson, Lower bounds for linear satisfiability problems (388--395).

John Hershberger and Subhash Suri, Morphing binary trees (396--404); Baruch Schieber, Computing a minimum-weight k -link path in graphs with the concave Monge property (405--411); Susanne Albers, Improved randomized on-line algorithms for the list update problem (412--419); William R. Burley and Sandy Irani, On algorithm design for metrical task systems (420--429); John Hershberger and Subhash Suri, Practical methods for approximating shortest paths on a convex polytope in \mathbb{R}^3 (447--456); Tomasz Radzik, Fast deterministic approximation for the multicommodity flow problem (486--492); Anil Kamath, Omri Palmon and Serge Plotkin, Fast approximation algorithm for minimum cost multicommodity flow (493--501); Anil Kamath and Omri Palmon, Improved interior point algorithms for exact and approximate solution of multicommodity flow problems (502--511); Bruce Hoppe and Eva Tardos, The quickest transshipment problem (512--521); Paolo Ferragina and Roberto Grossi, Fast incremental text editing (531--540).

Brenda S. Baker, Parameterized pattern matching by Boyer-Moore-type algorithms (541--550); Sampath Kannan, Z. Sweedyk and Steve Mahaney, Counting and random generation of strings in regular languages (551--557); Nabil Kahale and Tom Leighton [Frank Thomson Leighton], Greedy dynamic routing on arrays (558--566); Yonatan Aumann and Yuval Rabani, Improved bounds for all optical routing (567--576); James D. Fix and Richard E. Ladner, Optimal one-way sorting on a one-dimensional sub-bus array (586--594); Sampath Kannan and Tandy Warnow, A fast algorithm for the computation and enumeration of perfect phylogenies when the number of character states is fixed (595--603); John D. Kececioglu and R. Ravi, Of mice and men: algorithms for evolutionary distances between genomes with translocation (604--613); Vineet Bafna and Pavel Pevzner, Sorting permutations by transpositions (614--623); Martin Furer, Graph isomorphism testing without numerics for graphs of bounded eigenvalue multiplicity (624--631); David Eppstein, Subgraph isomorphism in planar graphs and related problems (632--640); Torben Hagerup, Jyrki Katajainen, Naomi Nishimura and Prabhakar Ragde, Characterizations of k -terminal flow networks and computing network flows in partial k -trees (641--649).

\{The papers of mathematical interest that appear to be in final form are being reviewed individually.\}

Reviewer: Editors

Review Type: Table of contents

Descriptors: *68-06 -Computer science (For papers involving machine computations and programs in a specific mathematical area, see Section --04 in that area)-Proceedings, conferences, collections, etc. ; 05-06 -Combinatorics (For finite fields, see 11Txx)-Proceedings, conferences, collections, etc.

22/5/50 (Item 3 from file: 239)

DIALOG(R) File 239:Mathsci

(c) 2003 American Mathematical Society. All rts. reserv.

01121278 MR 22##12005

Table look - up **procedures in language processing. I. The raw text .**
King, Gilbert W.
IBM J. Res. Develop.
1961, 5, 86--92
Language: English
Document Type: Journal
Subfile: MR (Mathematical Reviews) AMS
Abstract Length: LONG (43 lines)

This paper makes a strong case for the use of **table look - up** procedures in a variety of non-numerical **data** -processing applications. Although the techniques described are based specifically on a photographic memory developed by the author and various past and present associates, some of the ideas in the paper are likely to find **more** general applications. While much of the introductory part of the paper recapitulates some well-known properties of automatic storage media and of access procedures, several **new** techniques, of which the **table look - up** method of **address** modification is one of the most interesting, are presented. The storage of a dictionary for use in automatic language translation is used as an illustration.

The effect of certain difficulties on ultimately satisfactory exploitation of these techniques is insufficiently explored. While the author points out ``that dynamic dissection of words... can lead to errors'', his suggested remedy, ``to anticipate these peculiar cases, and enter the whole word'', is satisfactory only if anticipation is possible and practicable. It is not at all obvious that, for the very large tables the author contemplates storing, anticipation is possible. Indeed, the difficulties mentioned have led, in some experiments with the storage device not mentioned in the paper, to the production of English correspondents such as ``horsedensator'' and ``thatpenturoj'' for the Russian words ``kondensator'' and ``temperaturoj''. The presence or absence of these peculiar errors is a function of the current contents of the table, hence may vary from time to time. While the effect of such errors need not be serious, and while the remedy may work, no evidence is presented to the effect that a satisfactory solution has as yet been achieved.

In the matter of searching for long **addresses** through a splitting procedure and the use of prefixes, no mention is made of the procedure to be followed if not all parts can be **matched**. In this case, the information to be **matched** is no longer present in the input register. In connection with a similar problem arising in partial **matching**, it is mentioned that a subsequent paper in this series ``will elaborate the use of partial **matching** and show how the skipped information can be retrieved''; presumably the same thing will be done for the case of long **address** mismatches.

In spite of these shortcomings, however, it is not unlikely that the proposed techniques will find a significant range of satisfactory applications; they therefore deserve careful study.

Reviewer: Oettinger, A. G.

Descriptors: *94.00 -INFORMATION AND COMMUNICATION, CIRCUITS, AUTOMATA-General ; 68.00 -COMPUTING MACHINES-General

22/5/51 (Item 1 from file: 6)
DIALOG(R) File 6:NTIS
(c) 2003 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1268176 NTIS Accession Number: PB86-877107

Adaptive Communication. 1970-October 1986 (Citations from the NTIS Database)

(Rept. for 1970-Oct 86)

National Technical Information Service, Springfield, VA.

Corp. Source Codes: 055665000

Oct 86 132p

Languages: English Document Type: Bibliography

Journal Announcement: GRAI8626